

South Peak 15" Schematics

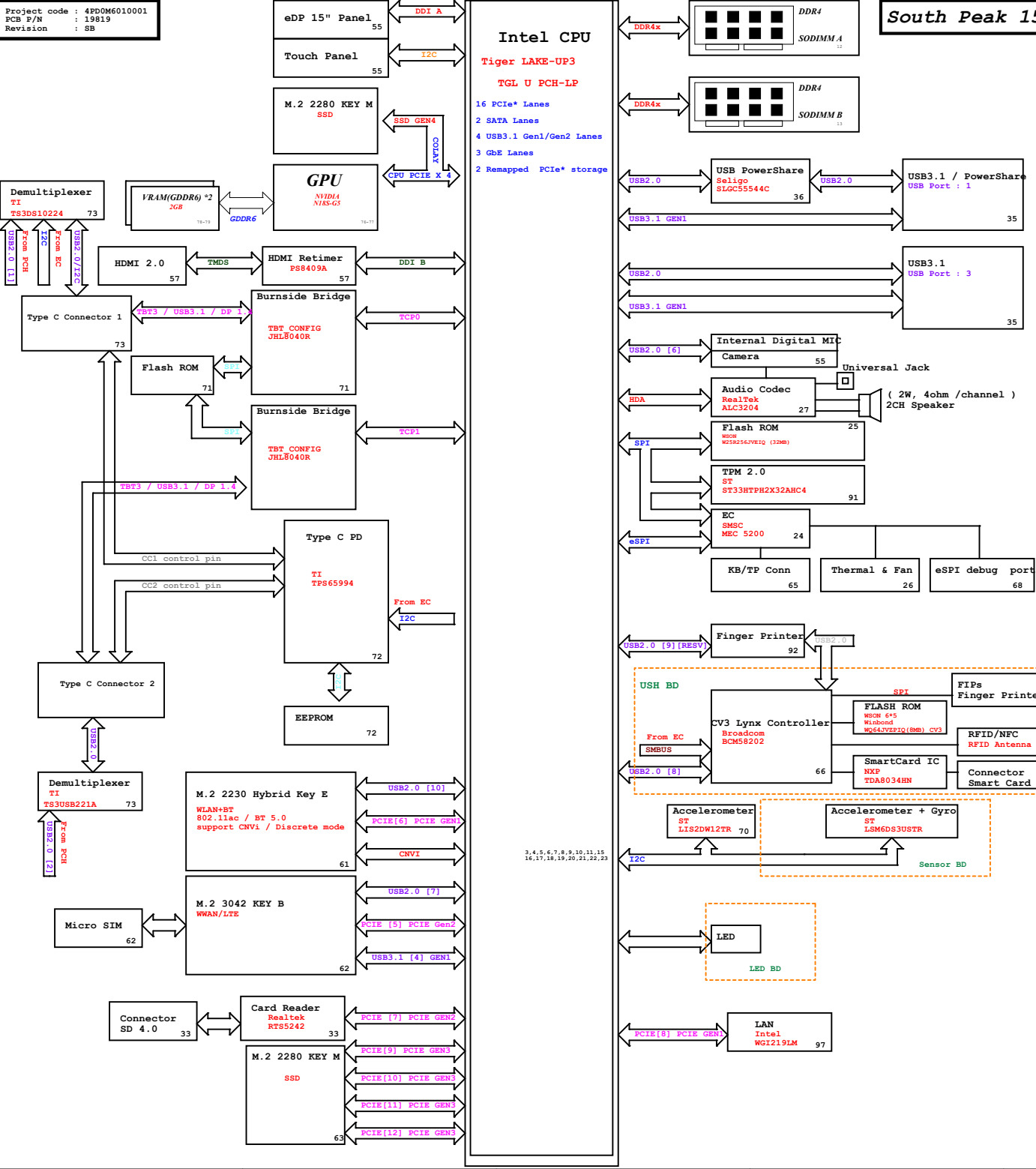
Tiger Lake-UP3

2020-04-24

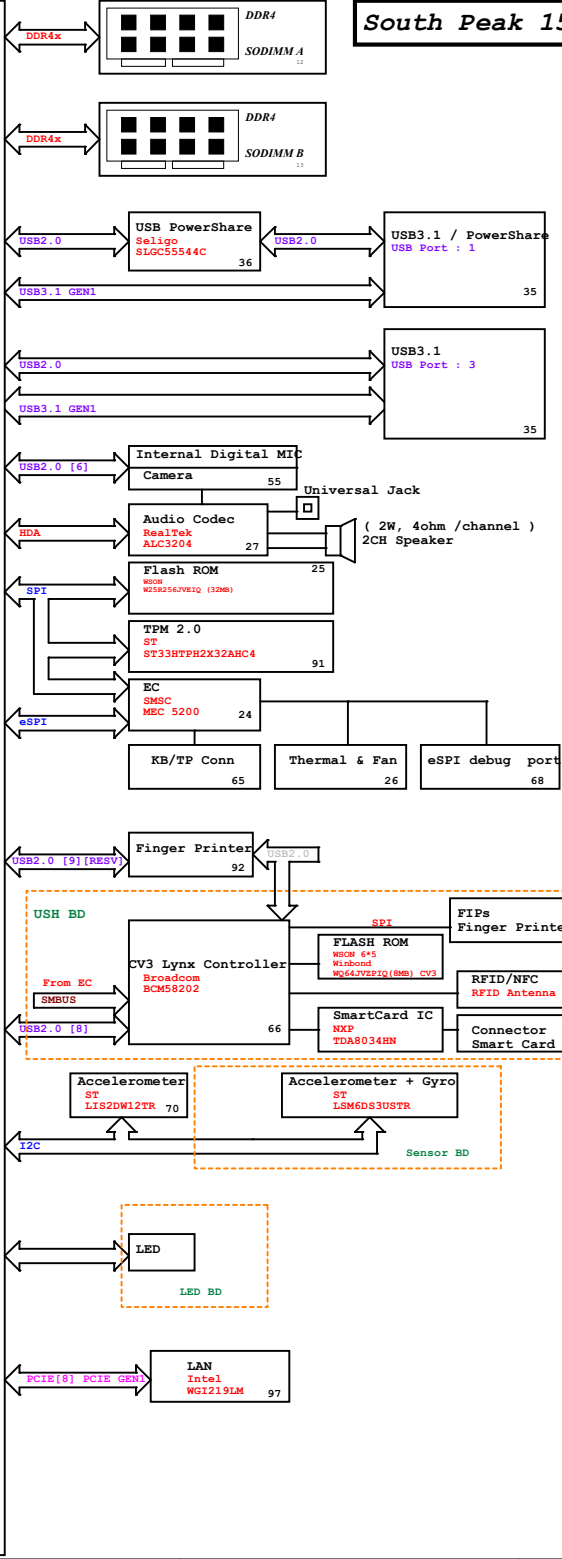
REV: SB

Multi

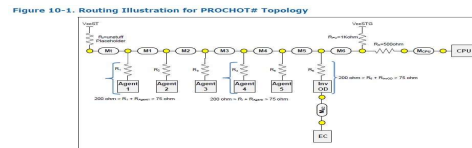
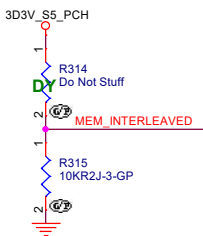
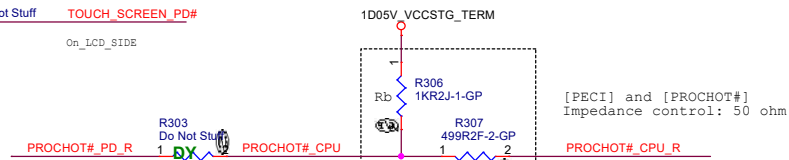
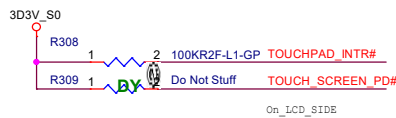
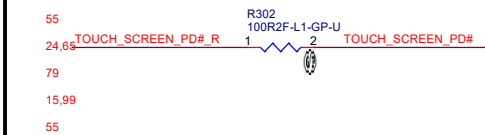
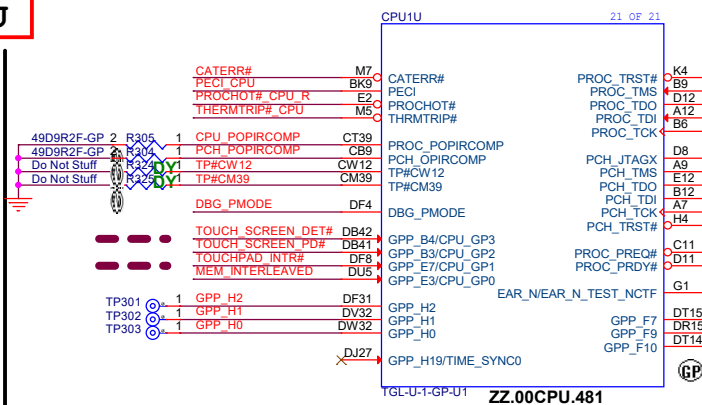
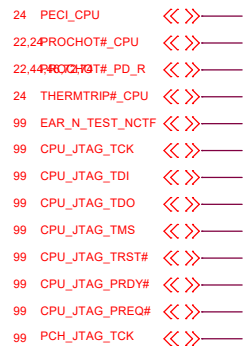
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Cover Page			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 1 of	106



South Peak 15" Block Diagram



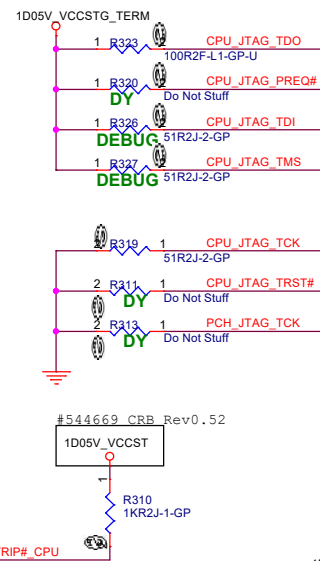
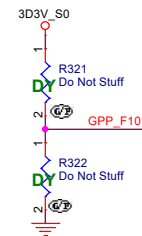
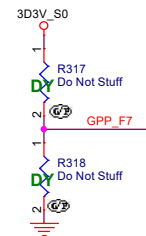
Main Func = CPU



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route (M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

DIMM TYPE

LOW	HIGH
NON_INTERLEAVED	INTERLEAVED



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Type

CPU (THML/JTAG)

Size
A3

Document Number

SouthPeak15 TGL

Rev
SB

Date: Friday, April 24, 2020

Sheet 3 of 106

Main Func = CPU

eDP

eDP_TX_CPU_N0 <<< 55
eDP_TX_CPU_P0 <<< 55
eDP_TX_CPU_N1 <<< 55
eDP_TX_CPU_P1 <<< 55
eDP_TX_CPU_N2 <<< 55
eDP_TX_CPU_P2 <<< 55
eDP_TX_CPU_N3 <<< 55
eDP_TX_CPU_P3 <<< 55

55 eDP_AUX_CPU_N <<< 55
55 eDP_AUX_CPU_P <<< 55

EDP_HPDI >>> 55
eDP_BLEN_CPU <<< 55
eDP_BLCtrl_CPU <<< 55
eDP_VDDEN_CPU <<< 55

USB_OC1# >>> 35

DP to MUX

DP2_DDI_TX_N0 <<< 57
DP2_DDI_TX_P0 <<< 57
DP2_DDI_TX_N1 <<< 57
DP2_DDI_TX_P1 <<< 57
DP2_DDI_TX_N2 <<< 57
DP2_DDI_TX_P2 <<< 57
DP2_DDI_TX_N3 <<< 57
DP2_DDI_TX_P3 <<< 57

DP_HPDI_CPU <<< 57

57CPU_DP2_CTRL_CLK <<< 57
57CPU_DP2_CTRL_DATA <<< 57

KB_DET# <<< 65

TBT2_LS_X0_RXD <<< 4,15,71

71 USB1_TCSS_RX_P1 <<< 71
71 USB1_TCSS_RX_N1 <<< 71
71 USB1_TCSS_RX_P0 <<< 71
71 USB1_TCSS_RX_N0 <<< 71
71 USB1_TCSS_TX_P1 <<< 71
71 USB1_TCSS_TX_N1 <<< 71
71 USB1_TCSS_TX_P0 <<< 71
71 USB1_TCSS_TX_N0 <<< 71
71 USB1_TCSS_AUX_P <<< 71
71 USB1_TCSS_AUX_N <<< 71

71 USB2_TCSS_RX_P1 <<< 71
71 USB2_TCSS_RX_N1 <<< 71
71 USB2_TCSS_RX_P0 <<< 71
71 USB2_TCSS_RX_N0 <<< 71
71 USB2_TCSS_TX_P1 <<< 71
71 USB2_TCSS_TX_N1 <<< 71
71 USB2_TCSS_TX_P0 <<< 71
71 USB2_TCSS_TX_N0 <<< 71
71 USB2_TCSS_AUX_P <<< 71
71 USB2_TCSS_AUX_N <<< 71

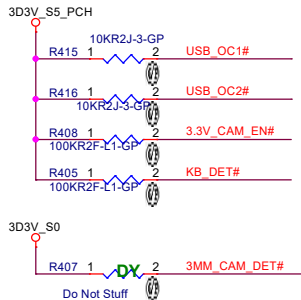
71 TBT_LS_X0_TXD <<< 71
15,71TBT_LS_X0_RXD <<< 71
71 TBT2_LS_X0_TXD <<< 71
4,15,71TBT2_LS_X0_RXD <<< 71

3.3V_CAM_EN# <<< 40

HDMI 2.0

TBT

CY20 CPU_DISP_HPDI4

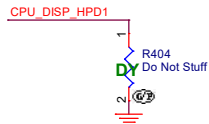


CPU1A

1 OF 21

eDP_TX_CPU_P3 AC2
eDP_TX_CPU_N3 AC1
eDP_TX_CPU_P2 AD2
eDP_TX_CPU_N2 AD1
eDP_TX_CPU_P1 AF1
eDP_TX_CPU_N1 AF2
eDP_TX_CPU_P0 AG2
eDP_TX_CPU_N0 AG1
eDP_AUX_CPU_P AJ2
eDP_AUX_CPU_N AJ1
DDIA_TXP3 DDIA_TXN3
DDIA_TXP2 DDIA_TXN2
DDIA_TXP1 DDIA_TXN1
DDIA_TXP0 DDIA_TXN0
DDIA_AUX_P DDIA_AUX_N
GPP_E22/DDPA_CTRLCLK/DNX_FORCE_RELOAD
GPP_E23/DDPA_CTRLDATA
EDP_HPDI DR5
GPP_E14/DDSP_HPDI4/DISP_MISCA
DP2_DDI_TX_P3 T12
DP2_DDI_TX_N3 T11
DP2_DDI_TX_P0 Y9
DP2_DDI_TX_N0 Y9
DP2_DDI_TX_P1 T9
DP2_DDI_TX_N1 P9
DP2_DDI_TX_P2 V11
DP2_DDI_TX_N2 V9
DDIB_TXP3 DDIB_TXN3
DDIB_TXP2 DDIB_TXN2
DDIB_TXP1 DDIB_TXN1
DDIB_TXP0 DDIB_TXN0
DDIB_AUX_P DDIB_AUX_N
GPP_H16/DDPB_CTRLCLK/PCIE_LNK_DOWN
GPP_H17/DDPB_CTRLDATA
DP_HPDI_CPU DG43
GPP_A18/DDSP_HPDI4/DISP_MISCB/I2S4_RXD
3.3V_CAM_EN# DG47
KB_DET# DJ47
GPP_A21/DDPC_CTRLCLK/I2S5_TXD
GPP_A22/DDPC_CTRLDATA/I2S5_RXD
TBT_LS_X0_TXD DU8
TBT_LS_X0_RXD DV8
GPP_E18/DDP1_CTRLCLK/TBT_LS_X0_TXD
GPP_E19/DDP1_CTRLDATA/TBT_LS_X0_RXD
TBT2_LS_X0_TXD DF6
TBT2_LS_X0_RXD DD6
GPP_E20/DDP2_CTRLCLK/TBT_LS_X1_TXD
GPP_E21/DDP2_CTRLDATA/TBT_LS_X1_RXD
GPP_D9/ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LS_X2_TXD/GSPI2_CS0#
GPP_D10/ISH_SPI_CLK/DDP3_CTRLCLK/TBT_LS_X2_RXD/GSPI2_CLK
GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LS_X3_TXD/GSPI2_MISO
GPP_D12/ISH_SPI_MOSI/DDP4_CTRLCLK/TBT_LS_X3_RXD/GSPI2_MOSI
GPP_A17/DISP_MISCC/I2S4_TXD
GPP_A19/DDSP_HPDI1/DISP_MISC1/I2S5_SCLK
GPP_A20/DDSP_HPDI2/DISP_MISC2/I2S5_SFRRM
USB_OC1# DH52
USB_OC2# DK45
GPP_A14/USB_OC1#/DDSP_HPDI3/I2S3_RXD/DISP_MISC3/DMIC_CLK_B1
GPP_A15/USB_OC2#/DDSP_HPDI4/DISP_MISC4/I2S4_SCLK
eDP_VDDEN_CPU DM8
eDP_BLEN_CPU DN8
eDP_BLCtrl_CPU DG10
EDP_VDDEN
EDP_BLCtrl
EDP_BLCtrl

TGL-U1-GP-U1
ZZ.00CPU.481



TCP0_TXRX_P1 AY2
TCP0_TXRX_N1 AY1
TCP0_TXRX_P0 BB1
TCP0_TXRX_N0 BB2
TCP0_TX_P1 AM5
TCP0_TX_N1 AM7
TCP0_TX_P0 AT7
TCP0_TX_N0 AT5
TCP0_AUX_P AP7
TCP0_AUX_N AP5
USB1_TCSS_RX_P1
USB1_TCSS_RX_N1
USB1_TCSS_RX_P0
USB1_TCSS_RX_N0
USB1_TCSS_TX_P1
USB1_TCSS_TX_N1
USB1_TCSS_TX_P0
USB1_TCSS_TX_N0
USB1_TCSS_AUX_P
USB1_TCSS_AUX_N

TBT

TCP1_TXRX_P1 AT2
TCP1_TXRX_N1 AT1
TCP1_TXRX_P0 AU1
TCP1_TXRX_N0 AU2
TCP1_TX_P1 AD5
TCP1_TX_N1 AD7
TCP1_TX_P0 AH7
TCP1_TX_N0 AH5
TCP1_AUX_P AF7
TCP1_AUX_N AF5
USB2_TCSS_RX_P1
USB2_TCSS_RX_N1
USB2_TCSS_RX_P0
USB2_TCSS_RX_N0
USB2_TCSS_TX_P1
USB2_TCSS_TX_N1
USB2_TCSS_TX_P0
USB2_TCSS_TX_N0
USB2_TCSS_AUX_P
USB2_TCSS_AUX_N

TBT2

TCP2_TXRX_P1 BF1
TCP2_TXRX_N1 BF2
TCP2_TXRX_P0 BE1
TCP2_TXRX_N0 BE2
TCP2_TX_P1 BD7
TCP2_TX_N1 BD5
TCP2_TX_P0 AY5
TCP2_TX_N0 AY7
TCP2_AUX_P BB5
TCP2_AUX_N BB7

TCP3_TXRX_P1 BK1
TCP3_TXRX_N1 BJ2
TCP3_TXRX_P0 BJ1
TCP3_TXRX_N0 BM7
TCP3_TX_P1 BM5
TCP3_TX_N1 BM6
TCP3_TX_P0 BH7
TCP3_TX_N0 BK5
TCP3_AUX_P BK7
TCP3_AUX_N BK8

TC_RCOMP_P AN2
TC_RCOMP_N AN1
DSI_DE_TE_2 M8
DDI_RCOMP AB1
DISP_UTILS/DSI_DE_TE_1 CE4

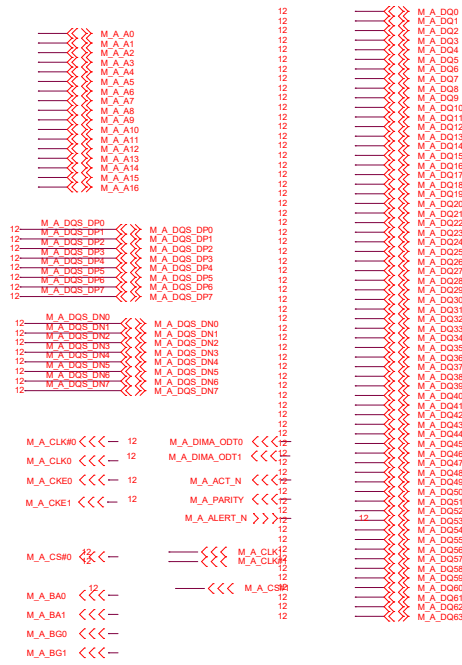


www.teknisi-indonesia.com

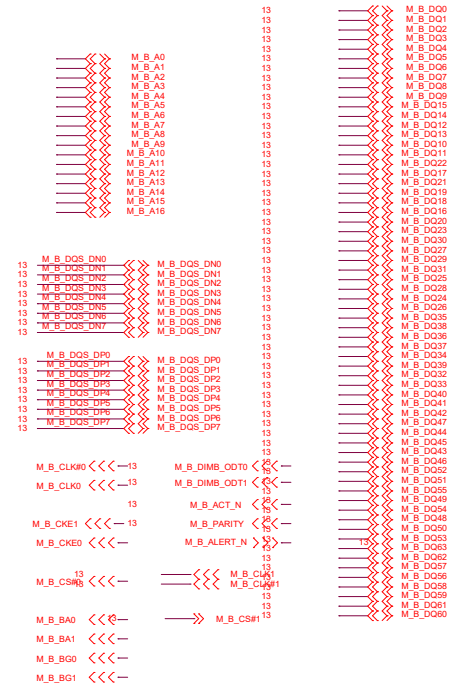
Multi

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: CPU (DDI/EDP)			
Size: A3	Document Number: SouthPeak15 TGL	Rev: SB	
Date: Friday, April 24, 2020	Sheet: 4	of	106

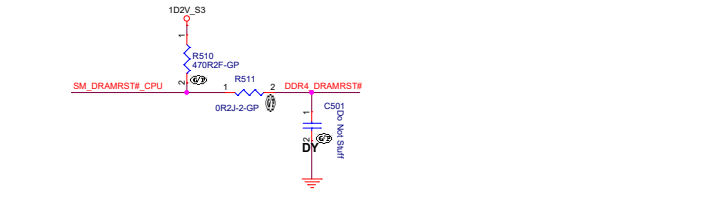
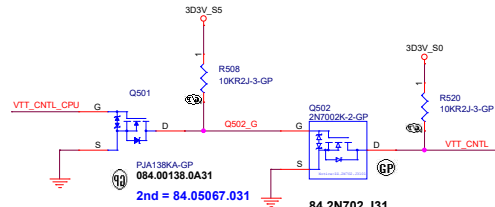
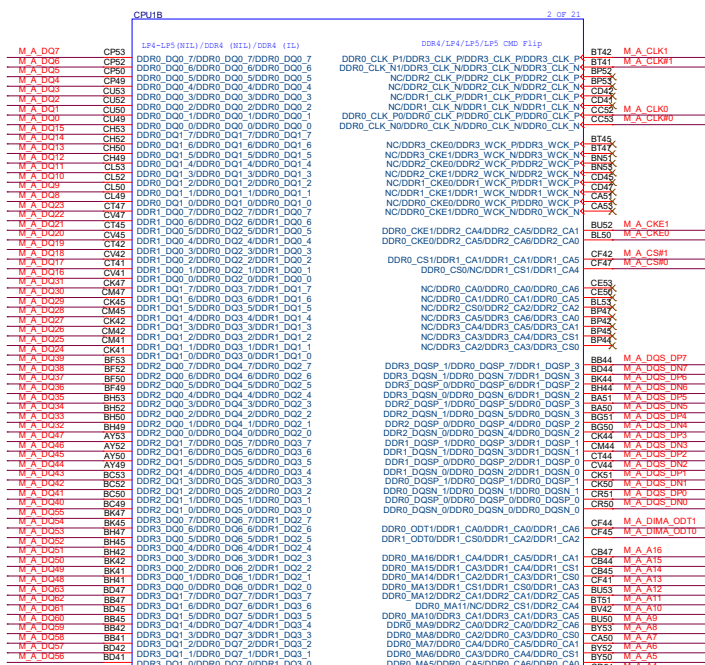
Channel A



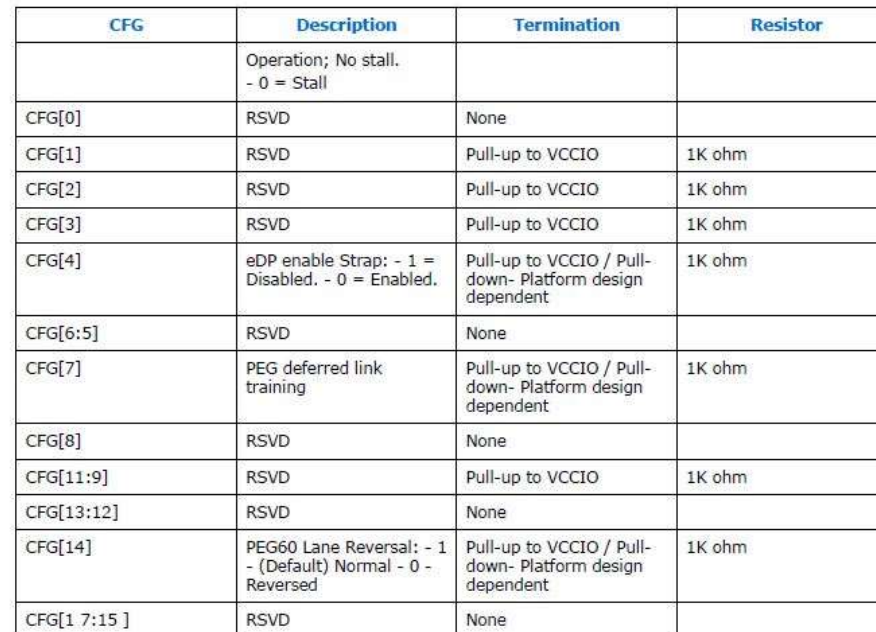
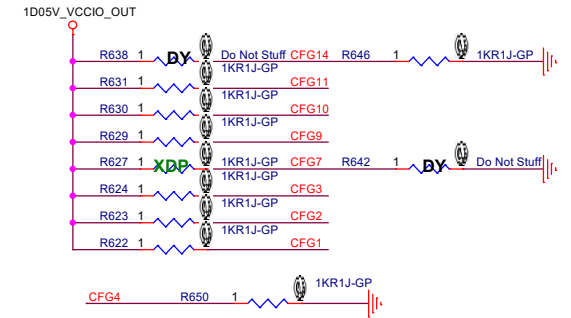
Channel B



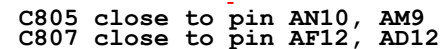
DDR4 ball type: Non-Interleaved Type



CFG0	<< >>	99
CFG1	<< >>	99
CFG2	<< >>	99
CFG3	<< >>	99
CFG4	<< >>	99
CFG5	<< >>	99
CFG6	<< >>	99
CFG7	<< >>	99
CFG8	<< >>	99
CFG9	<< >>	99
CFG10	<< >>	99
CFG11	<< >>	99
CFG12	<< >>	99
CFG13	<< >>	99
CFG14	<< >>	99
CFG15	<< >>	99
CFG16	<< >>	99
CFG17	<< >>	99
BPM_N1	<<< —	99
BPM_N0	<<< —	99



www.teknisi-indonesia.com



21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Rev
SE

Sheet 8 of 106

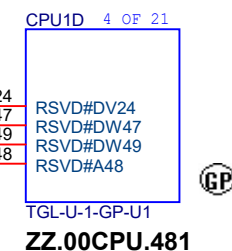
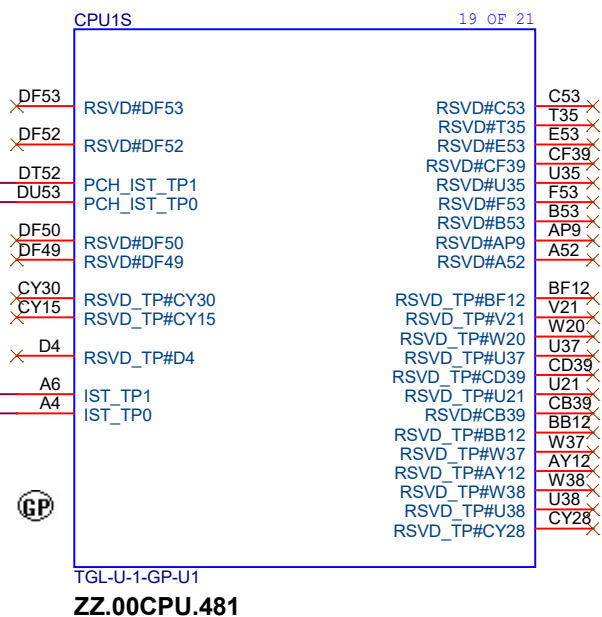
607872 Ver0.9 page350 Optional

607872 Ver0.9 page350 recommend

20190430_Byron



20190430_Byron

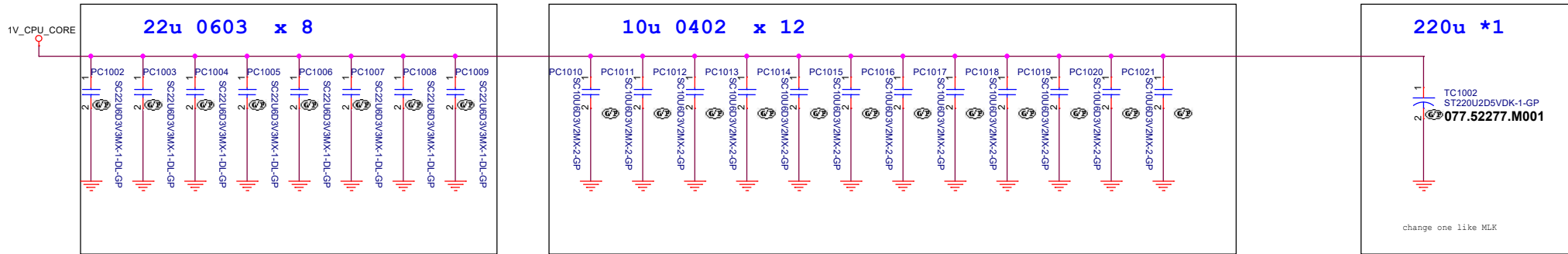


Multi

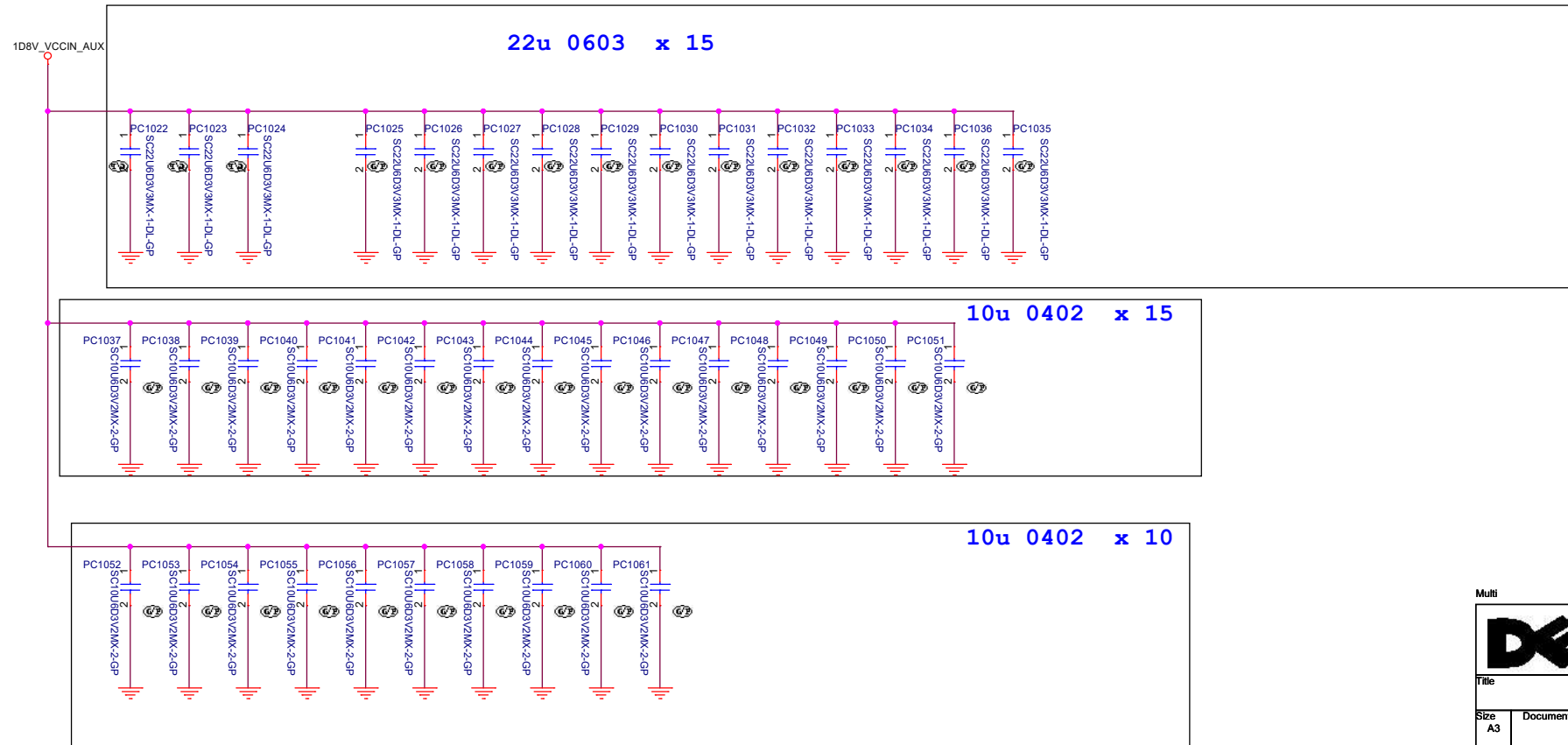
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU (RSVD)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 9 of	106

Main Func = CPU

1V_CPU_CORE (VCCIN)



VCCIN_AUX



Multi



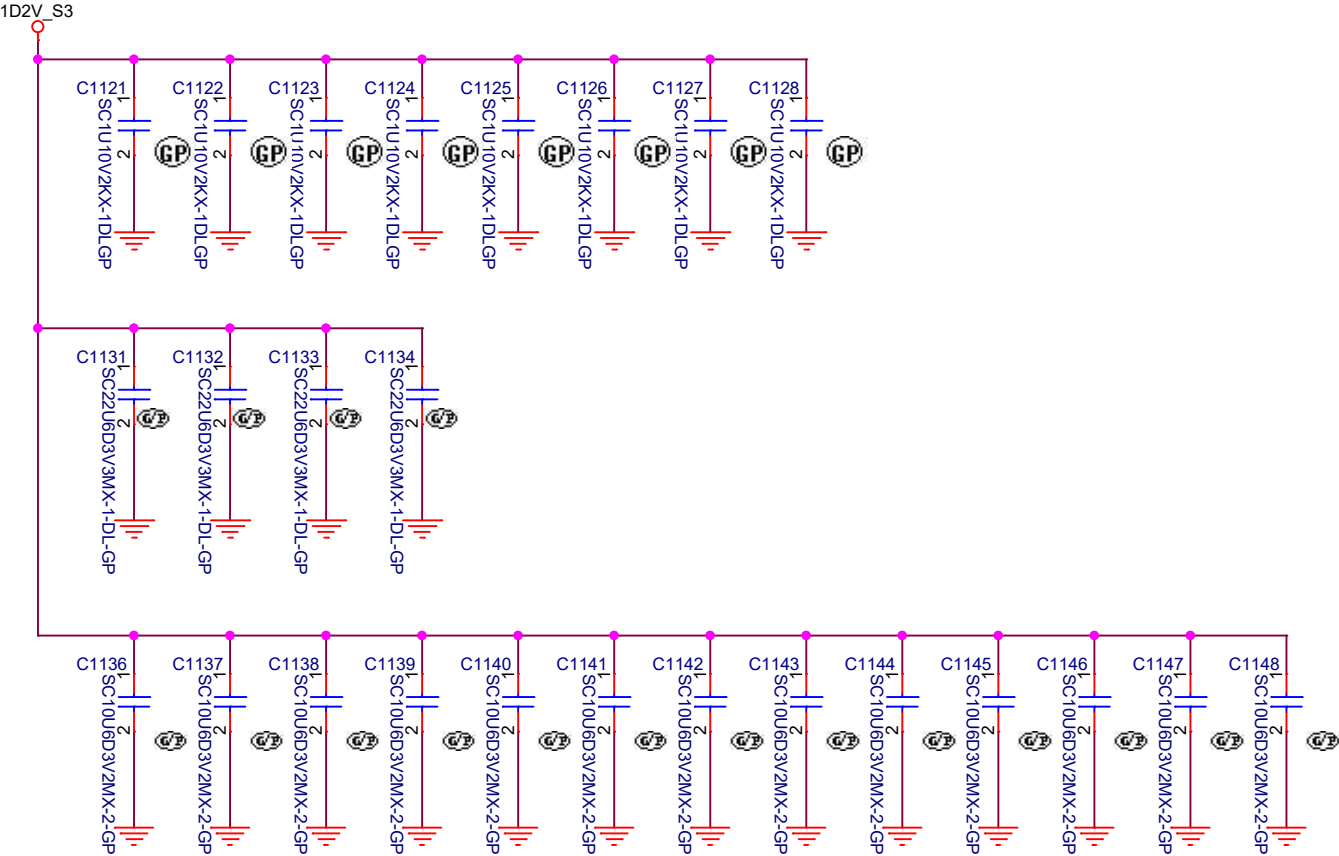
Title CPU (CORE Power Cap1)

Size A3 Document Number SouthPeak15 TGL Rev SB

Date: Friday, April 24, 2020 Sheet 10 of 106

Main Func = CPU

VDDQ



Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU (Power Cap2)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 11 of	106

(Blanking)

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title DDR (RSVD) (DDR4-CHA1)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 14	of 106

18.6899 SPI_SI_CPU <<<—
18.6899 WP_CPU <<<—
18.68SPI_HOLD_CPU <<<—

CNV_RGL_DT >>>—
GPP_C5 <<<—
GPP_E6 <<<—
HDA_SDO <<<—
TBT_LSX0_RXD >>>—

3.99 DBG_PMODE <<<—
4.71 TBT2_LSX0_RXD <<<—
18 GPP_E10 <<<—

GPIO	GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK (GPP_R2)	CNVI debug MODES (GPP_F2)	
21.61				=20K PD=		* PH as VCCPGPPR =20K PD=, 1D8V_GPPR_S5, R1509, ME_UNLOCK1, HDA_SDO, R1515 DR2J-2-GP, Do Not Stuff		
Schematic	High	ESPI Disable	Disable	Enable	19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)	Disable	OVERRIDEN	INTEGRATED CNVI DISABLE
	Low	Enable =default=	Enable	Disable	38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)	Enable	SECURITY MEASURES NOT OVERRIDEN	INTEGRATED CNVI ENABLE
GPIO	TBT LSX VCCIO conf. #0	TBT LSX VCCIO conf. #1	TBT LSX VCCIO conf. #2	TBT LSX VCCIO conf. #3	A0		GPP_E10	GPP_E11
Schematic	E19	E21	D10	D12				
	High	3.3V	3.3V	3.3V	3.3V	Disable	DFXTESTMODE DISABLED (DEFAULT)	
Low	1.8V	1.8V	1.8V	1.8V	Enable	DFXTESTMODE ENABLED		

Original Ref.

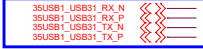
GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK	M.2 CNVI MODES	TBT LSX #0
ESPI OR EO LESS HIGH: ESPI IS DISABLED LOW: ESPI SELECTED WEAK INTERNAL PU 20K	BOOT HALT HIGH - DISABLED LOW: ENABLED NO INTERNAL PUPD	JTAG ODT DISABLE LOW: JTAG ODT DISABLED HIGH: JTAG ODT ENABLED NO INTERNAL PUPD	CPU/SSC CLOCK FREQ HIGH: 19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL) LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT) WEAK INTERNAL PU 20K	CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PUPD	FLASH DESCRIPTOR SECURITY OVERRIDE HIGH: OVERRIDEN LOW: SECURITY MEASURES NOT OVERRIDEN WEAK INTERNAL PU 20K	M.2 CNVI MODES LOW-> INTEGRATED CNVI ENABLE HIGH-> INTEGRATED CNVI DISABLE NO INTERNAL PUPD	TBT LSX #0 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PUPD
TBT LSX #1	TBT LSX #2	TBT LSX #3	A0	GPP_E10	GPP_E11		
TBT LSX #1 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PUPD	TBT LSX #2 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PUPD	TBT LSX #3 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PUPD	A0 PERSONALITY STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PUPD				

Main Func = PCH

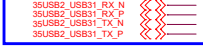
#543016:
220 nF nominal capacitors are recommended for Gen 3
100 nF nominal capacitors are recommended for Gen 2

(#545659) The xHCI controller supports USB Debug port on all USB3.0 capable ports.

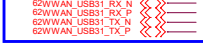
USB3.1 PORT1



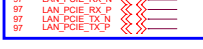
USB3.1 PORT2



WWAN



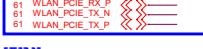
LAN



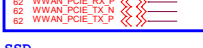
CARD



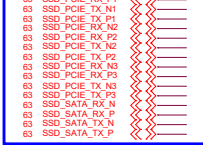
WLAN



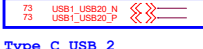
WWAN



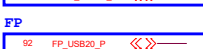
SSD



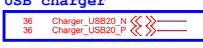
Type C USB 1



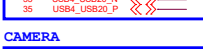
Type C USB 2



FP



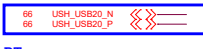
USB charger



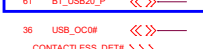
USB2.0 port4



CAMERA



WWAN



USH



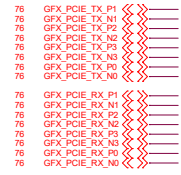
BT



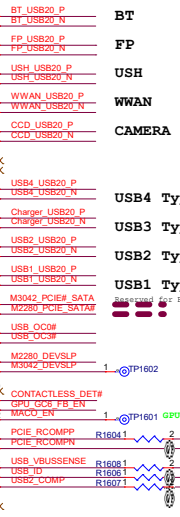
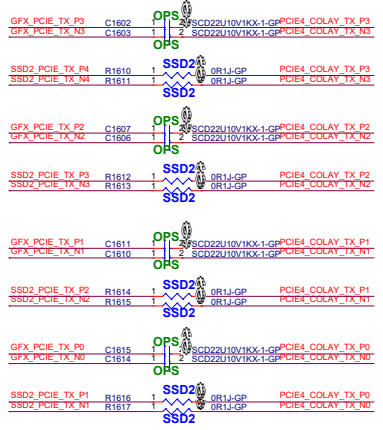
USB_OC3W



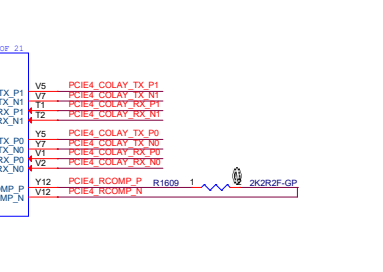
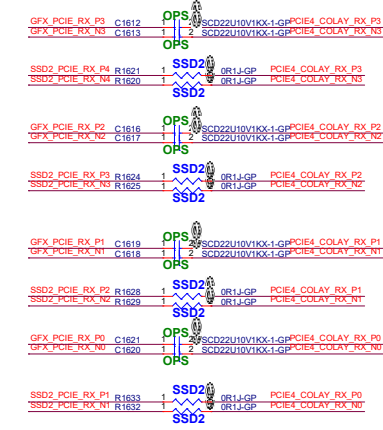
tekniisi indonesia



TGL-U1-GPU1
ZZ.00CPU.481



TGL-U1-GPU1
ZZ.00CPU.481



Layout Note:

1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

```

24.58 SIO_SLP_SUS#          <<<
68      SIO_SLP_SUS#       <<<
51.08   SIO_SLP_SUS#       <<<
24.40.68 SIO_SLP_S3#       <<<
68      SIO_SLP_S4#        <<<
68      SIO_SLP_S5#        <<<
68.90   SIO_SLP_S0#        <<<

40      SIO_SLP_LAN#       <<<
40      SIO_SLP_LAN#       <<<

68.99   SYS_RESET#        <<<

PCH_DPWROK
PCH_PWROK
SYS_PWROK_R                <<<

RTC_INTRUDET#             >>>

SIO_PWRBST#               >>>

24      AC_PRESENT         <<<

97      LAN_WAKE#          <<<

24.62   PCH_PCIE_WAKE#    <<<

97      PM_LANPHY_ENABLED <<<

97      RTCSTN_ON          >>>

RSMRSTN_KBC               <<<

ALL_SYS_PWRGD             <<<

33.61.68 SLP_TRST#_RIGHT <<<
63.71.76 PCH_PLTRST#_LEFT <<<

40.91   CPU_C10_GATE#     <<<

20.27   SPKR              <<<

40      VCCST_OVERRIDE    <<<
40      AC_DIS_ACP        >>>

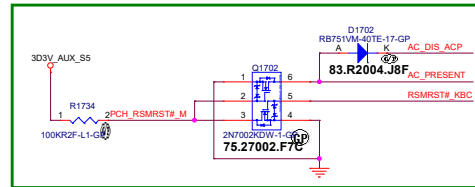
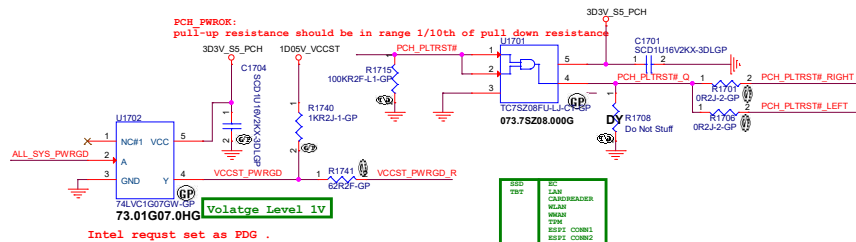
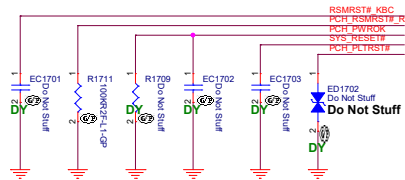
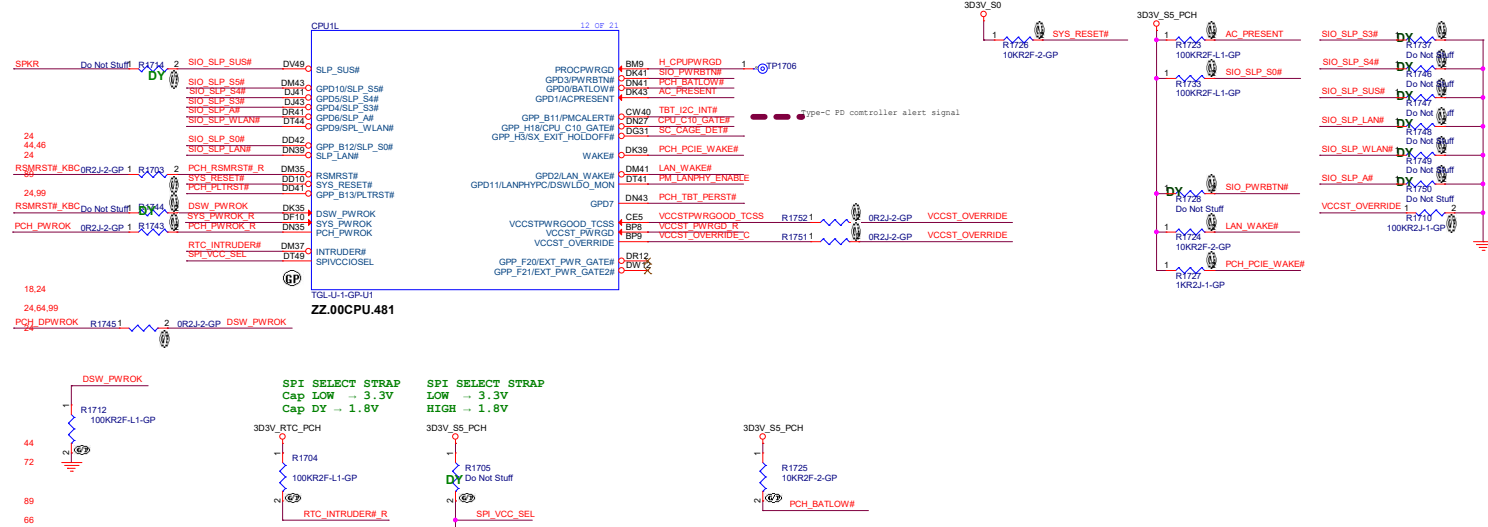
TBT_LCN_INT#              <<<

71      PCH_TBT_FERST#    <<<

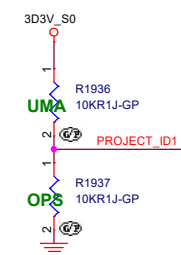
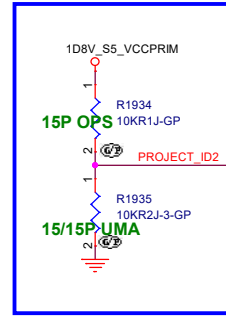
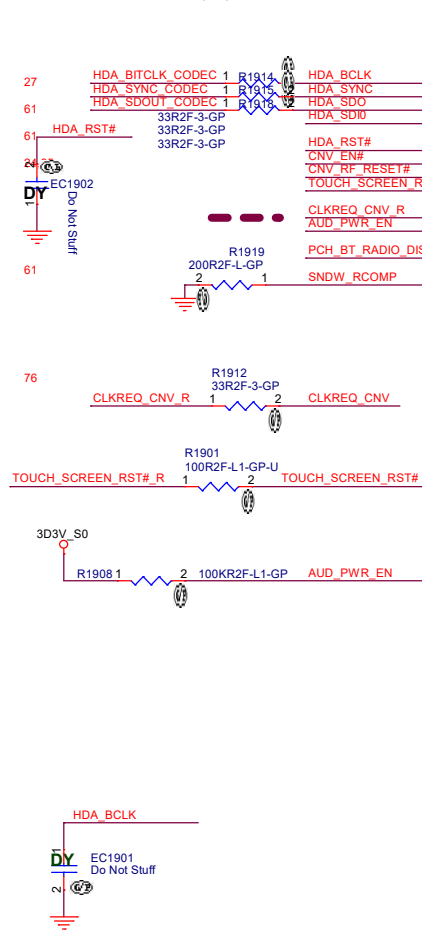
RTC_INTRUDET_R            >>>

SC_CAGE_DET#              <<<

```

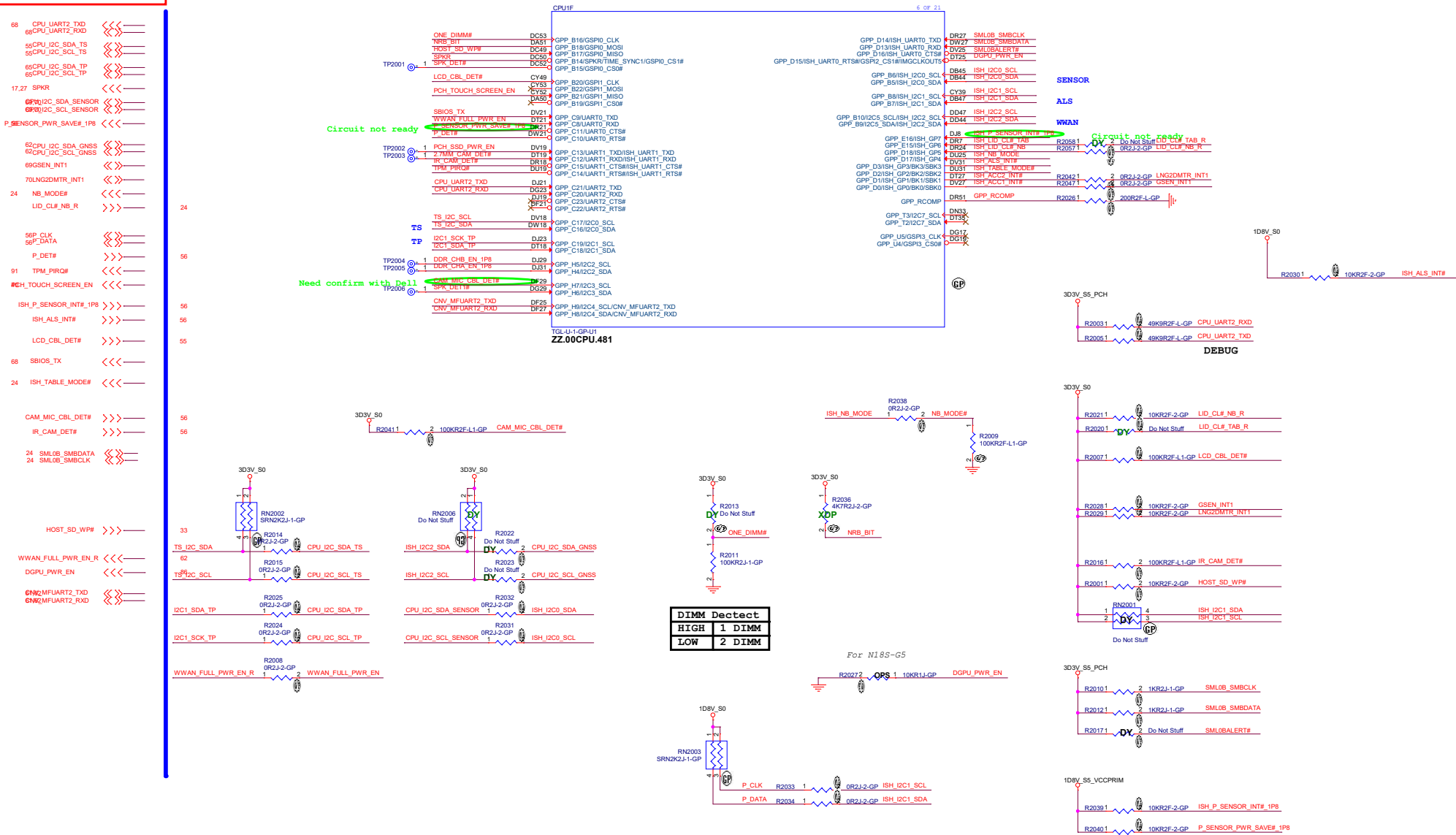


ME_FWP_PCH 1 R1904 1KR2J-1-GP HDA_SDO



ϕ^i	15 (i3, i5, i7) $^{2\phi}$		15P (i5, i7) $^{2\phi}$	
ϕ^i	UMA ϕ^i	DSC (N155-G5) ϕ^i	UMA ϕ^i	DSC (QN20-M1) $^{2\phi}$
Accelerometer sensor on MB $^{2\phi}$	LNG2DMTR (8-bit) $^{2\phi}$	LNG2DMTR ϕ^i	LNG2DMTR $^{2\phi}$	LIS2DW12TR (16-bit)$^{2\phi}$
GPP_RS (PROJECT_ID1) ϕ^i	1 ϕ^i	0 ϕ^i	1 ϕ^i	0 ϕ^i
GPP_S4 (PROJECT_ID2) ϕ^i	0 ϕ^i	0 ϕ^i	0 ϕ^i	1 ϕ^i

Main Func = PCH





1



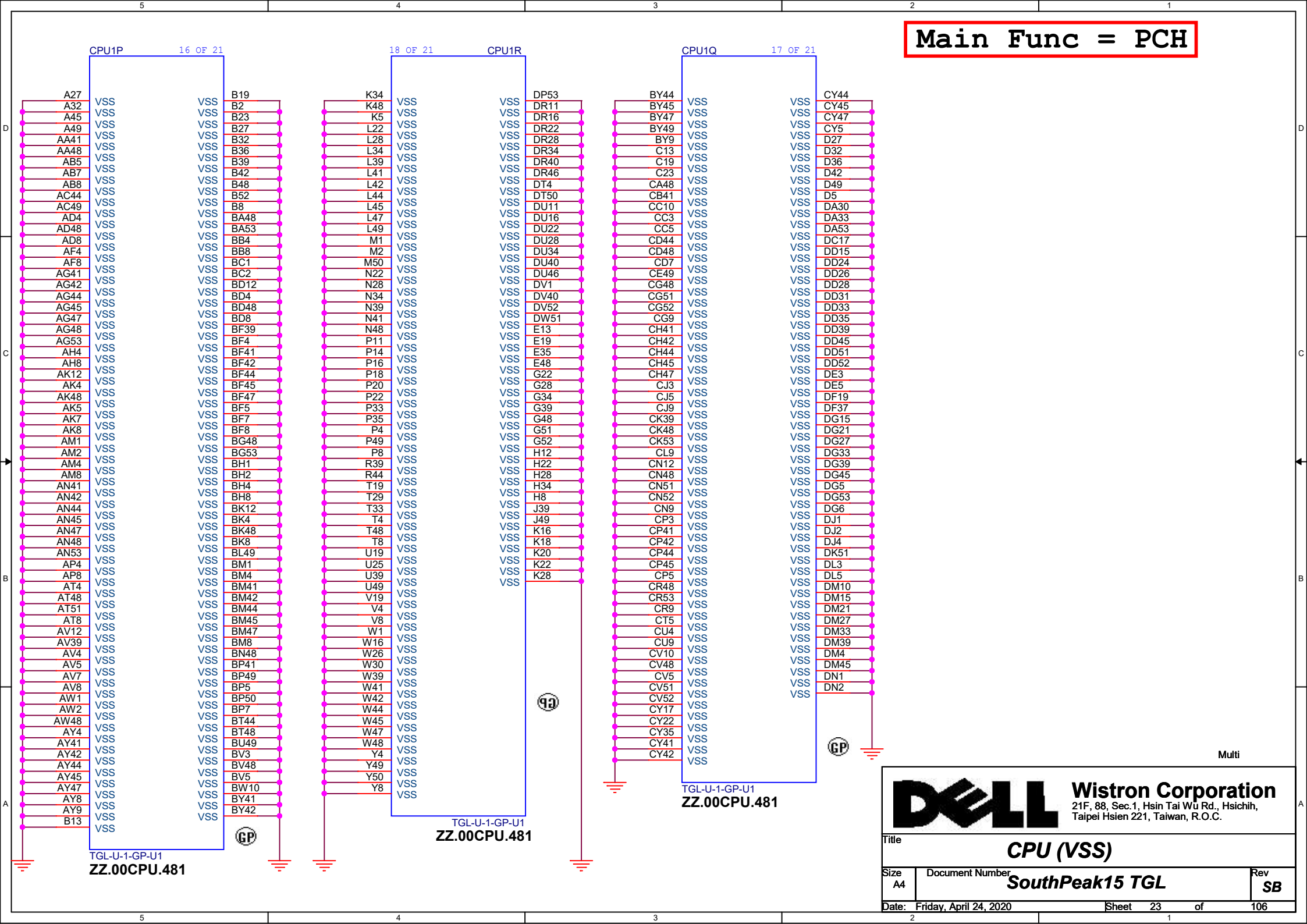
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

CPU (EMMC/CNVi)

SouthPeak15 TGL

Sheet 21 of 106

Main Func = PCH



Multi

DELL **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **CPU (VSS)**

Size A4	Document Number SouthPeak15 TGL	Rev SB
------------	---	------------------

Date: Friday, April 24, 2020 Sheet 23 of 106

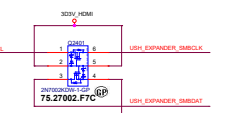
```

i-> EC ->RSMRST
.L ACT
RSMRST 50ms ,control DPWROK .
power down ,SLP SUS low DSW must be low .
比 SLP SUS 還早拉的時候一定要 DPWROK 也拉 .

```


 RC452
 100KΩF-2.1-GP
 ESPI_SHARE_BOOT_SELECT

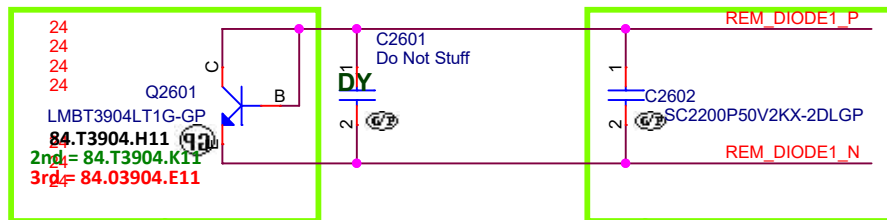
 RC456
 Do Not Stuff



Main Func = Thermal / FAN

REM_DIODE1_P
REM_DIODE1_N
REM_DIODE2_P
REM_DIODE2_N

REM_DIODE4_P
REM_DIODE4_N
PWM_FAN1
TACH_FAN1

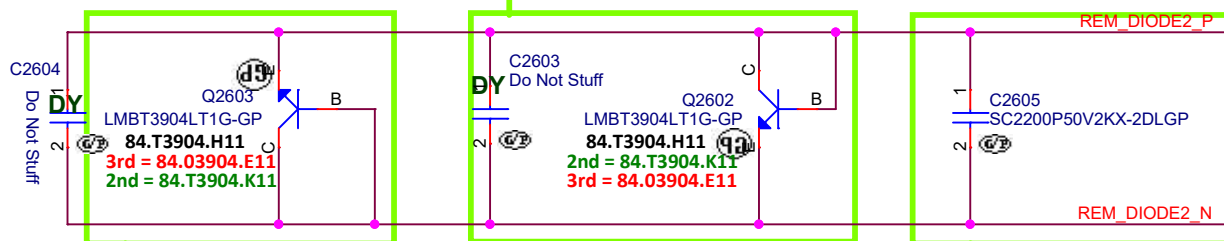


Layout Note: Place to CPU

Layout Note: Close to EC

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

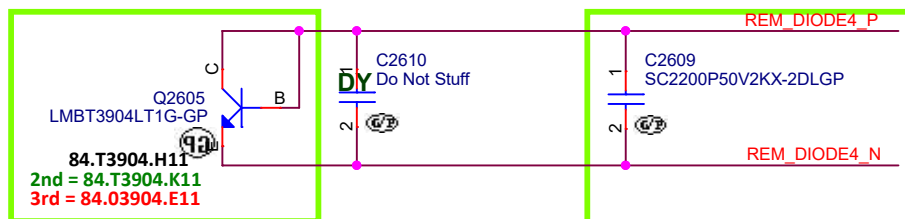
Layout Note: Close to WWAN/2nd SSD



Layout Note: Place to DIMM

Layout Note: Close to EC

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

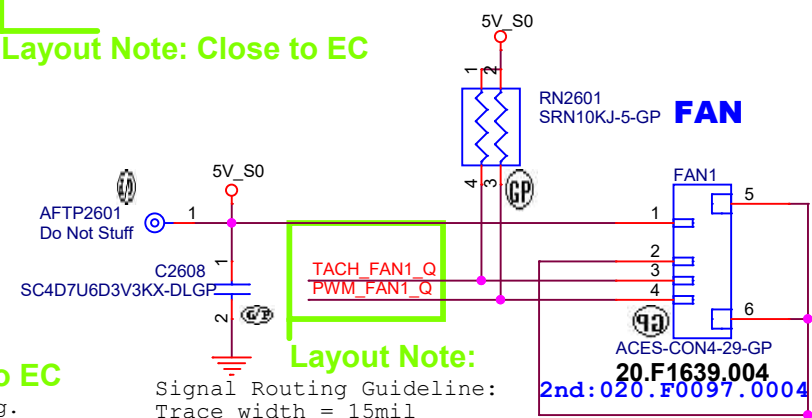
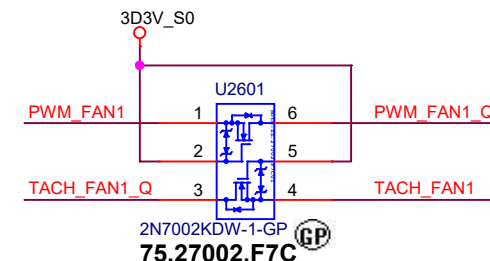


Layout Note: Place to V.R

Layout Note: Close to EC

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

5105 Channel	Location
DP1/DN1	CPU (Q2601)
DP2/DN2	WWAN (Q2602)
DN2a/DP2a	DDR (Q2603)
DP4/DN4	V.R (Q2605)



Layout Note:

Signal Routing Guideline:
Trace width = 15mil

TACH_FAN1_Q 1
PWM_FAN1_Q 1

AFTP2602 Do Not Stuff
AFTP2603 Do Not Stuff

Multi



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title INT IO (Thermal/Fan)

Size A4 Document Number SouthPeak15 TGL

Rev SB

Date: Friday, April 24, 2020

Sheet 26 of 106

5	4	3	2	1
D				
C				
B				
A				

Multi

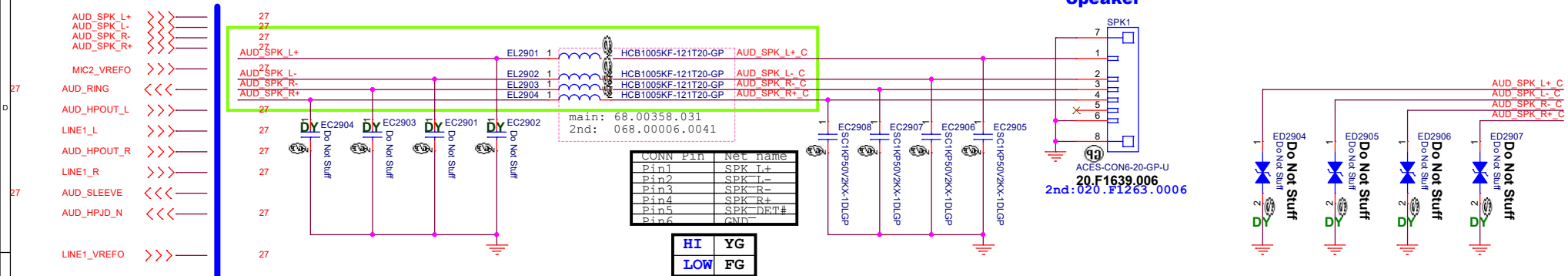
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Audio (RSVD) (Audio AMP)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 28	of 106

Main Func = Audio

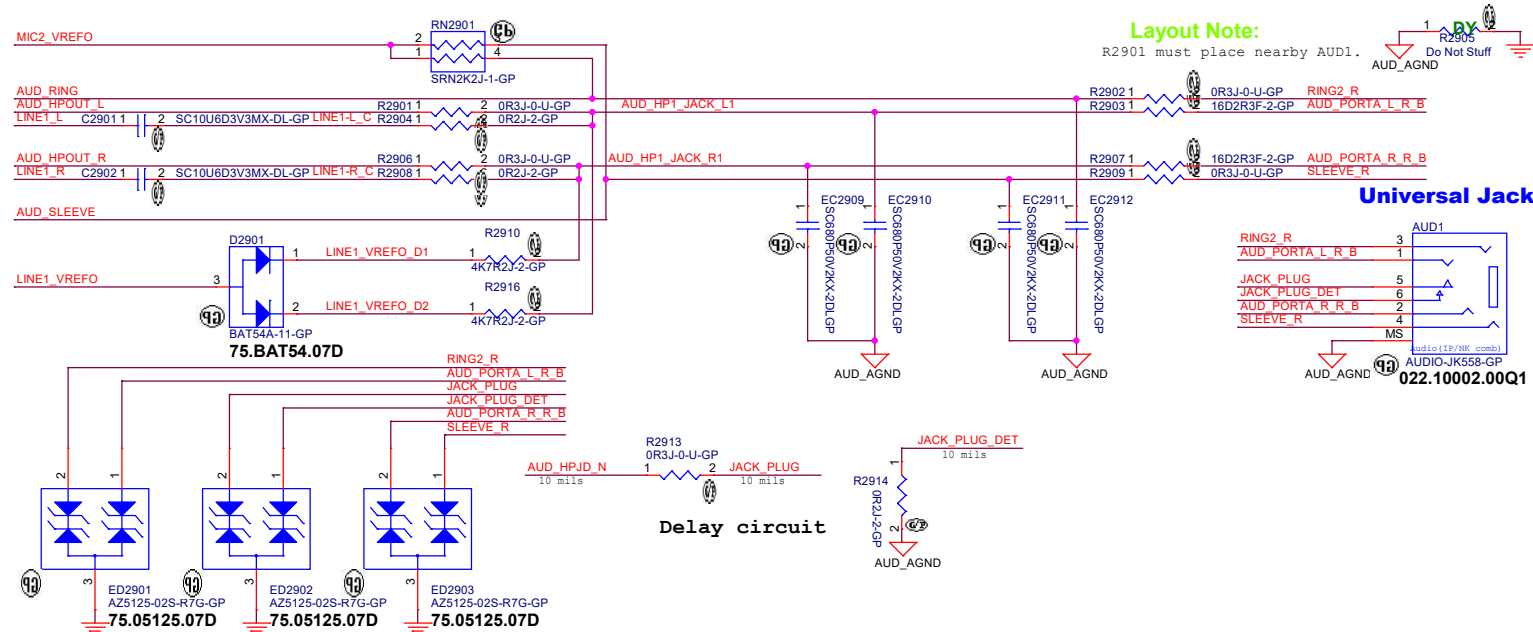
Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

Speaker



www.teknisi-indonesia.com



Multi

5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Audio (HP/SPK/MIC Jack)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 30 of	106

5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title LAN (RSVD)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 31	of 106

Main Func = LAN

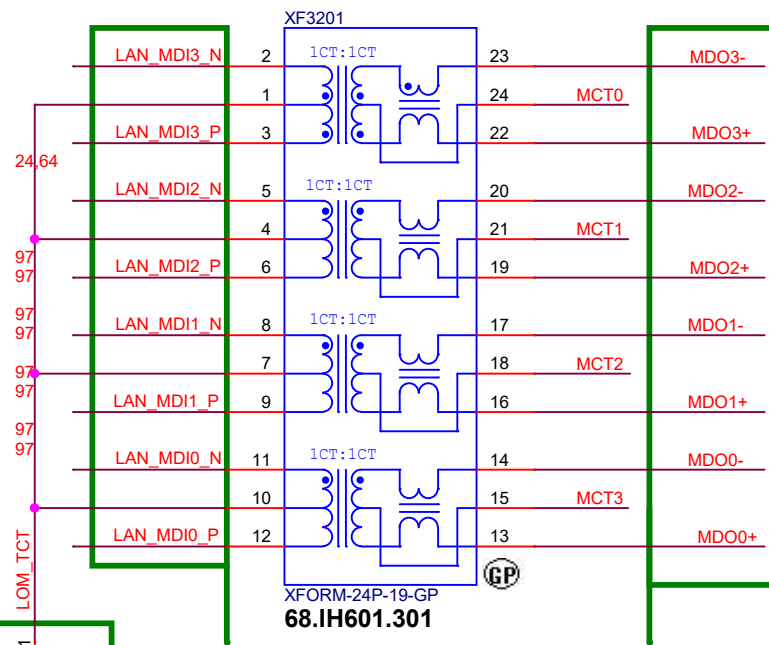
LED_MASK#
LAN_0_GREEN_LINK_N
LAN_1_AMBER_ACT_N

LAN_MDI0_P
LAN_MDI0_N

LAN_MDI1_P
LAN_MDI1_N

LAN_MDI2_P
LAN_MDI2_N

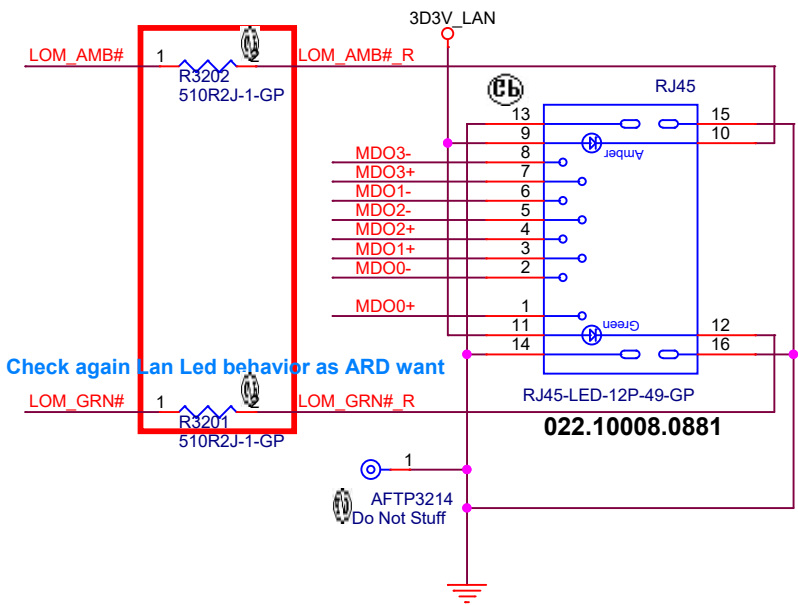
LAN_MDI3_P
LAN_MDI3_N



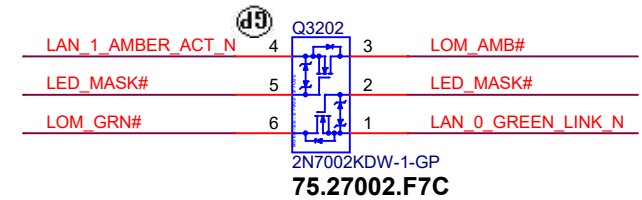
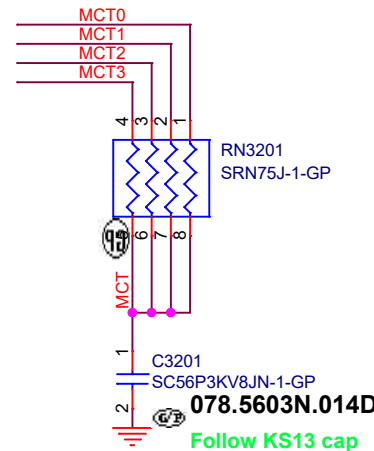
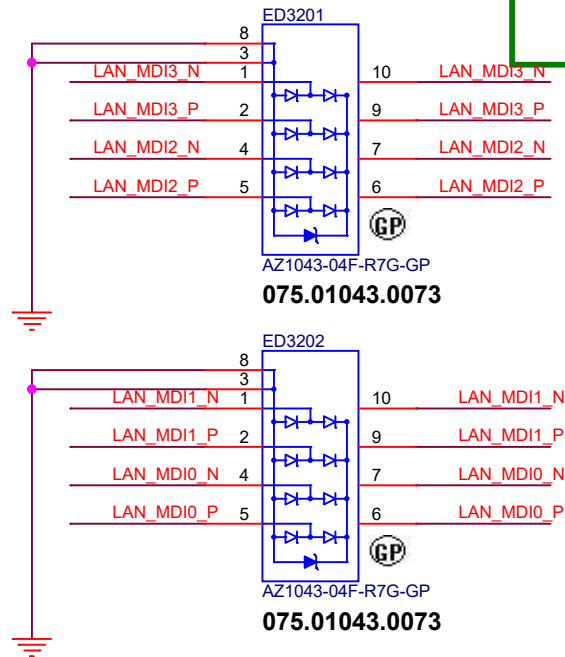
Layout note:
30 mil spacing between MDI differential pairs.

Follow Reference Schematic 0.01uF~0.4uF

Check again Lan Led behavior as ARD want



www.teknisi-indonesia.com



- LED0 (010): Green = Indicates Link connection established (located on left-hand side of connector)
- LED1 (011): Amber = Blinking when network activity (located on right-hand side of connector)

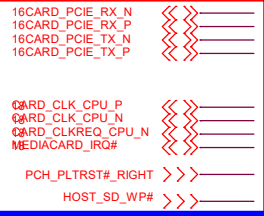
Multi

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title LAN (RSVD) (RJ45+Transformer)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 32	of 106

Main Func = Card Reader

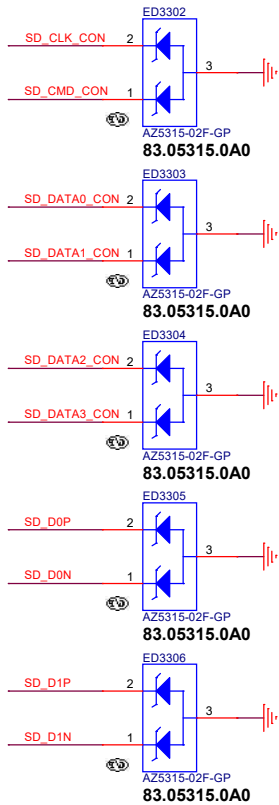
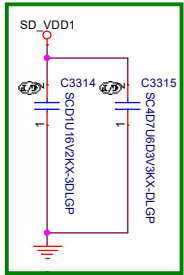
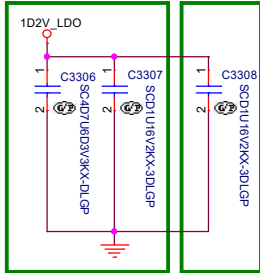
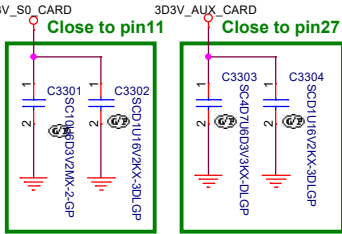
3D3V_S0_CARD

850mA

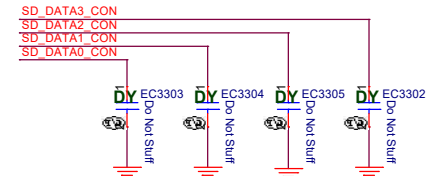
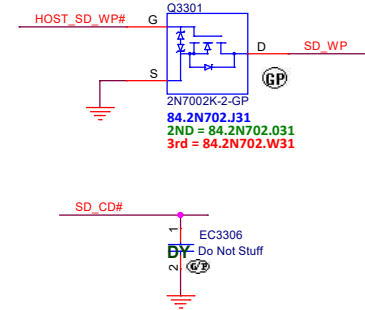
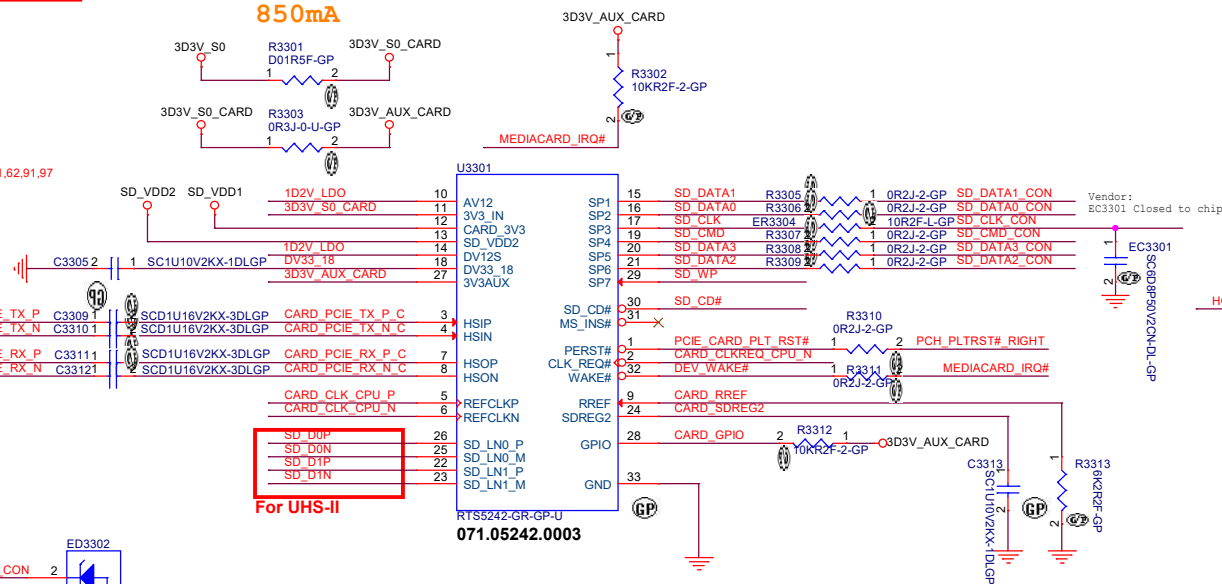
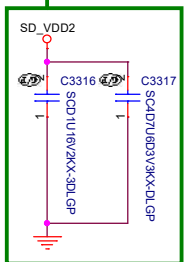


Layout Note:

17,61,62,91,97
20



Layout Note:Close to Card Reader CONN



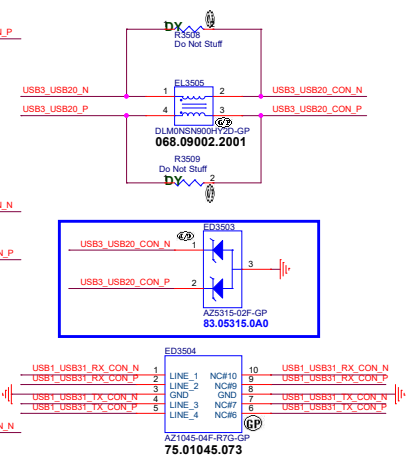
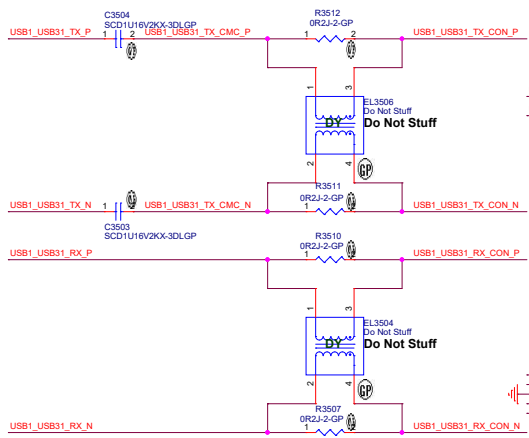
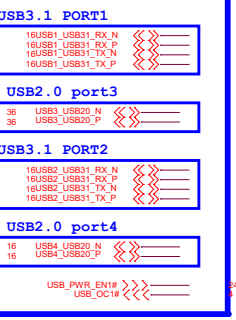
5	4	3	2	1
D				
C				
B				
A				

Multi

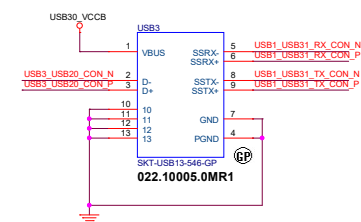
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title USB (RSVD) (USB2.0 CONN)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 34	of 106

Main Func = USB 3.0

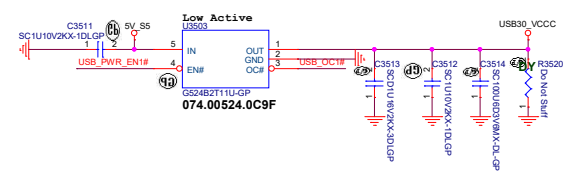
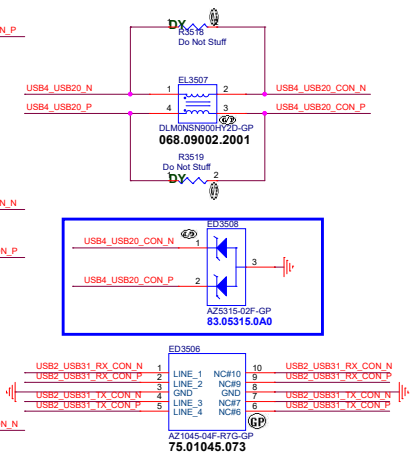
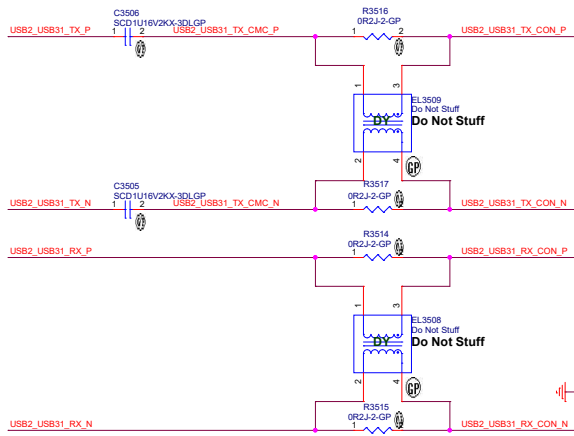
USB3/USB31-1/USB20-3/PowerShare



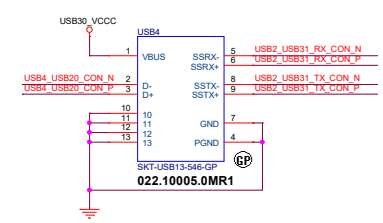
EXT Port1 Right Side, Support Power Share



USB4/USB31-2/USB20-4



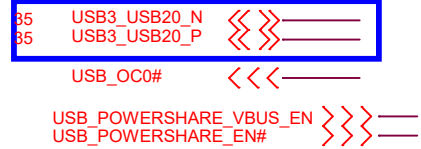
EXT Port1 Right Side, Support Power Share



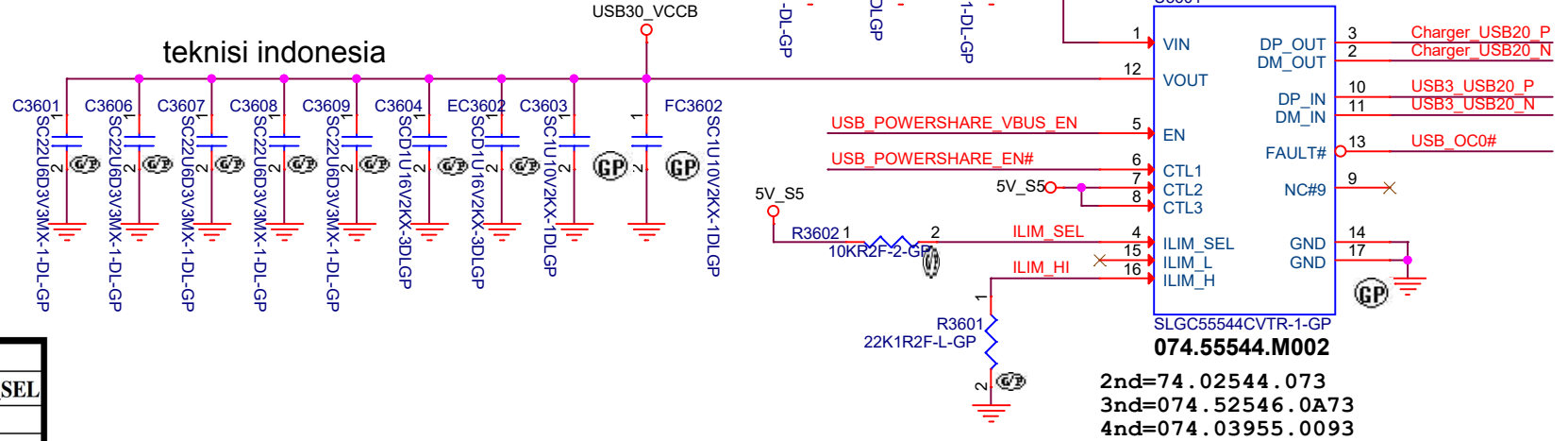
Main Func = USB Charger

support power share on the USB3.0 port on the right side of platform

USB2.0 port3



USB charger



Device Control Pins				
Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH(Discharge)	0	0	0	x
CDP	1	1	1	1
SDP2(No Discharge from/to CDP)	1	1	1	0
SDP1(Discharge from/to any charging state including CDP)	1	1	0	x
	0	1	0	x
DCP_Short	1	0	0	x
DCP/Divider-1A	1	0	1	x
DCP_Auto	0	1	1	x
	0	0	1	x

Current Limit	MIN	TPY	MAX
TI	2120	2275	2430
PERICOM	2120	2275	2430
NUVOTON	2235	2400	2570

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		USB (USB Charger)	
Title	Document Number		Rev
Size A4	SouthPeak15 TGL		SB
Date: Friday, April 24, 2020		Sheet 36 of 106	1

5	4	3	2	1
D				D
C				C
B				B
A				A

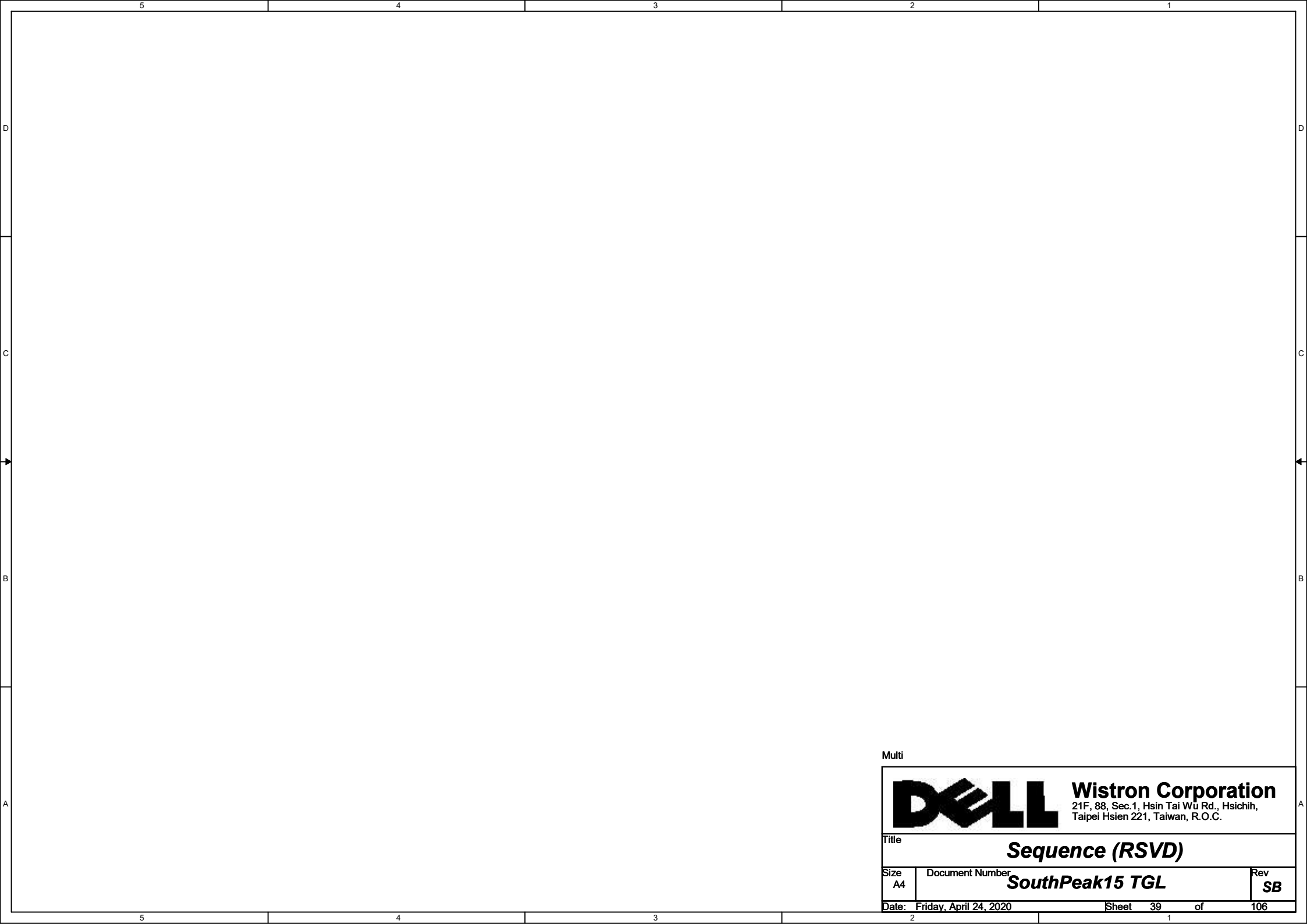
Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title USB (RSVD) (PCIE to USB3.0)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 37	of 106

5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

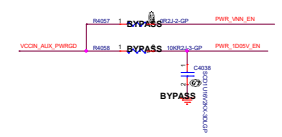
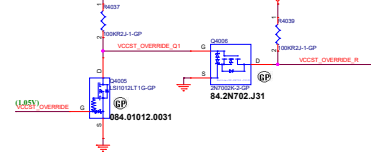
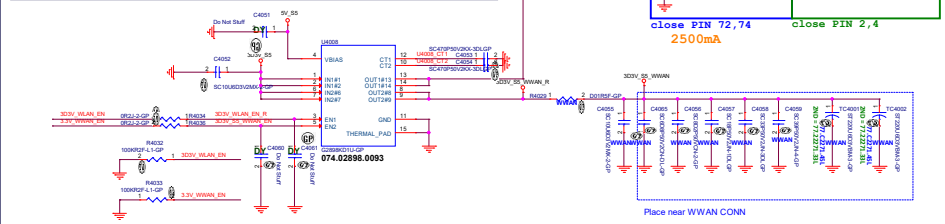
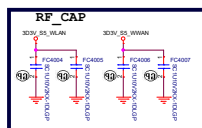
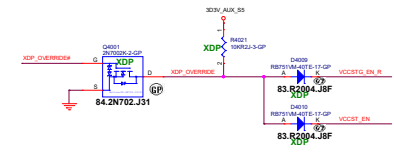
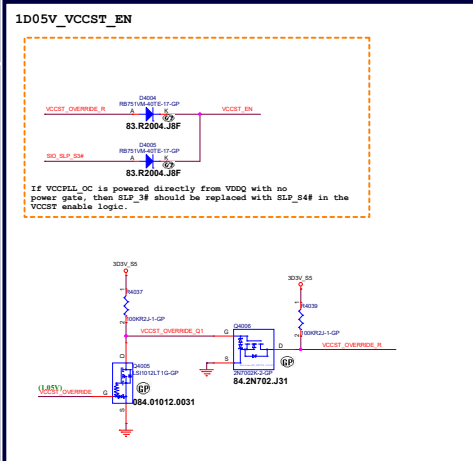
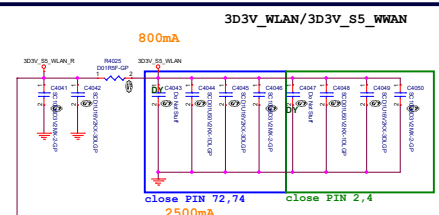
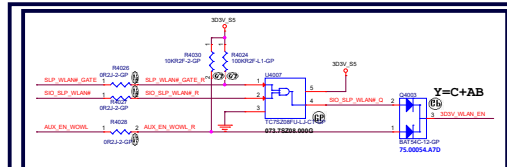
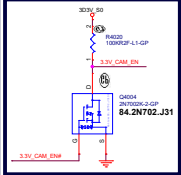
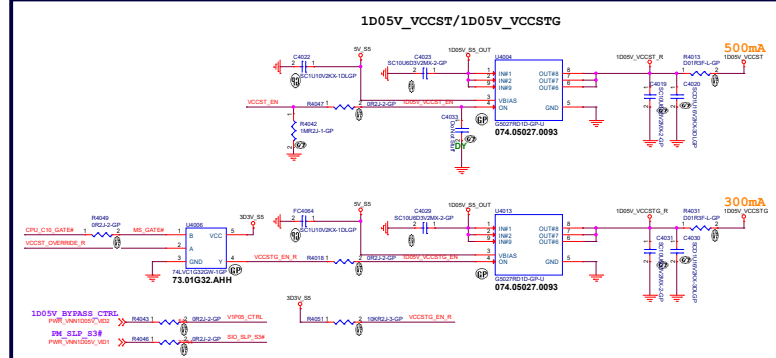
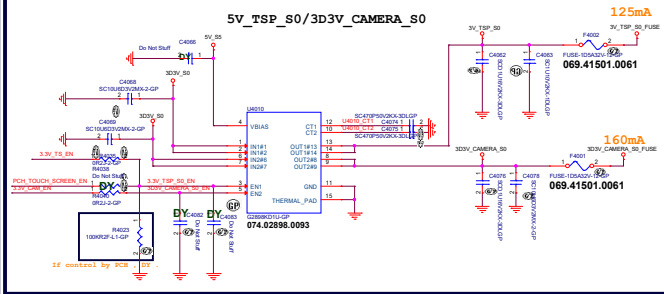
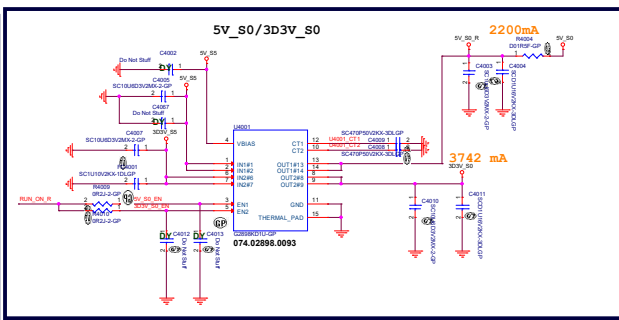
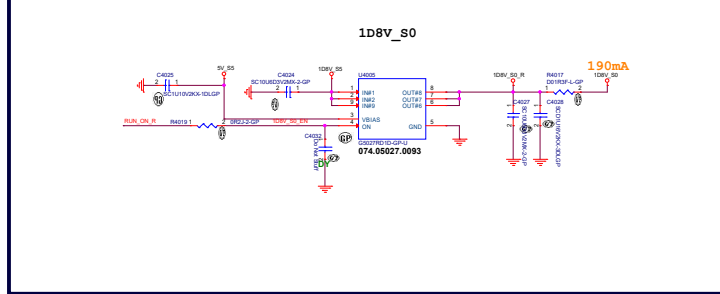
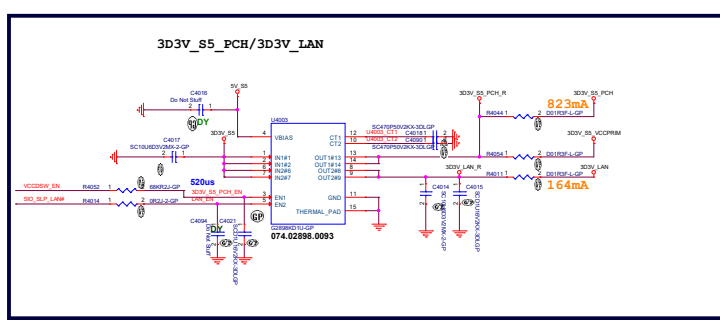
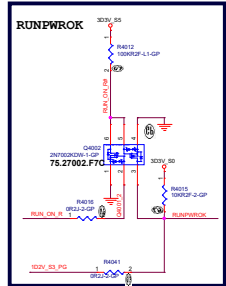
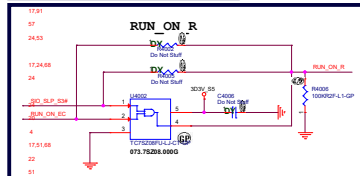
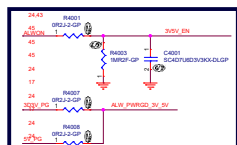
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title USB (RSVD) (USB Redriver/Hub)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 38	of 106



Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Sequence (RSVD)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 39	of 106

3WEN	>>>
3VW_EN	<<<
30DV_PG	>>>
3V_PG	>>>
ALW_PWRGD_3V_5V	>>>
SIO_SL_PAN	>>>
SLW_INW_GATE	>>>
SIO_SL_INWEN	>>>
ALX_EN_WGDL	>>>
3V_WVRN_EN	>>>
XDP_XDPEN#	>>>
CLK_C0_GATE#	>>>
RLN_C1_R	>>>
VCCDQW_EN	>>>
SIO_SL_53M	>>>
RLN_C0_R	>>>
RLNAPWR	>>>
3V_5V	>>>
TOUCH_SCREEN_EN	>>>
3V_CAM_EN	>>>
SIO_SL_54#	>>>
VPMPS_CTRL	>>>
10DV_53M	>>>
ESP_RESET#	>>>
VCCIN_ALW_PWRGD	>>>
PWR_NIN_EN	>>>
PWR_100V_EN	>>>
VCCST_OVRDRIVE	>>>
SS_PG	>>>
PWR_VOCAL_PG	>>>
PWR_INWEN_PG	>>>



5	4	3	2	1
D				
C				
B				
A				

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Sequence (RSVD) (DS3/S0ix)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 41	of 106

5	4	3	2	1
D				D
C				C
B				B
A				A

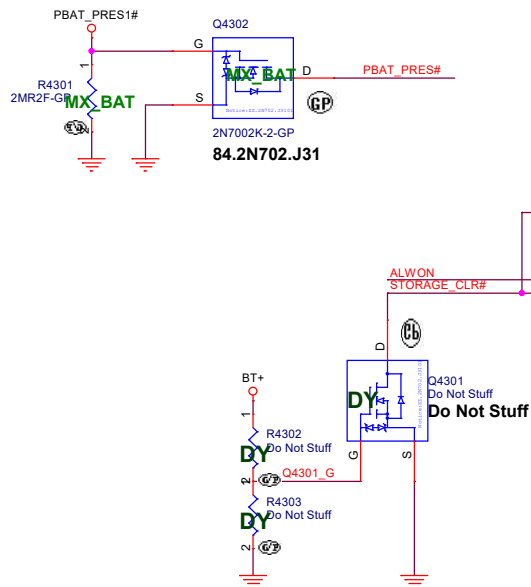
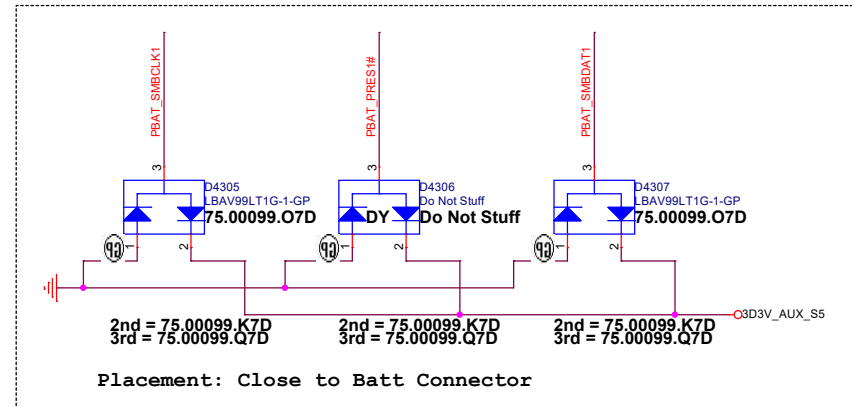
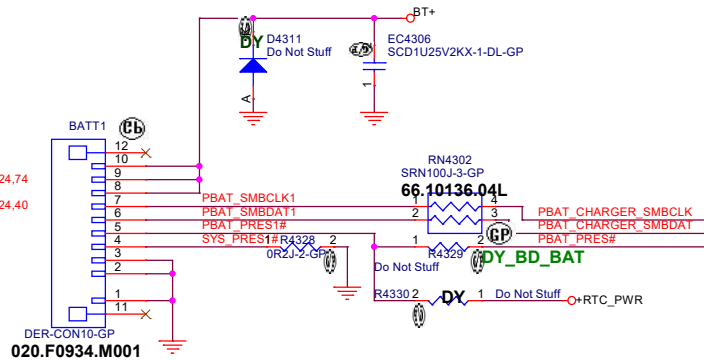
Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title INT IO (RSVD)			
Size A4	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020		Sheet 42 of	106

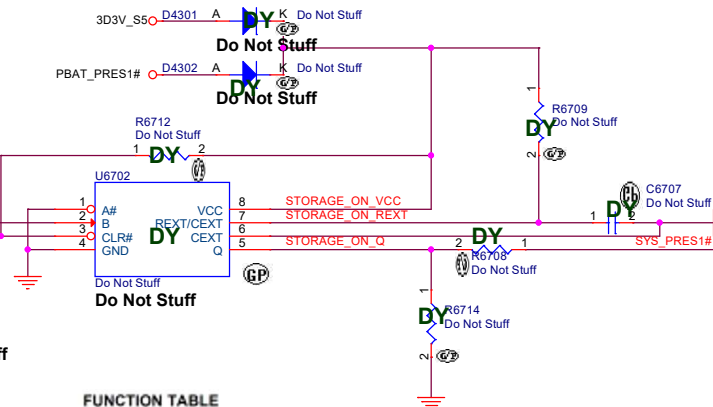
Main Func = BATT Com

AC_DIS >>> 24.44
DCIN1_EN >>> 24.74
PBA74.Q#IARGER_SMBCLK <<< 24.44
PBA74.Q#IARGER_SMBDAT <<< 24.44
PBAT_PRES# <<< 24.44,74
AC_DISC# <<< 24.44,74
VBUS2_ECOK >>> 24.74
ALWON >>> 24.40

Batt Connector



ADVANCED STORAGE MODE



FUNCTION TABLE

INPUTS			OUTPUTS
CLR	A	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	↑
H	↓	H	↓
↑	L	H	↓

Normal mode

ADVANCED STORAGE MODE Step1.

www.teknisi-indonesia.com

Multi



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DC IN/BATT Conn

Size

Document Number

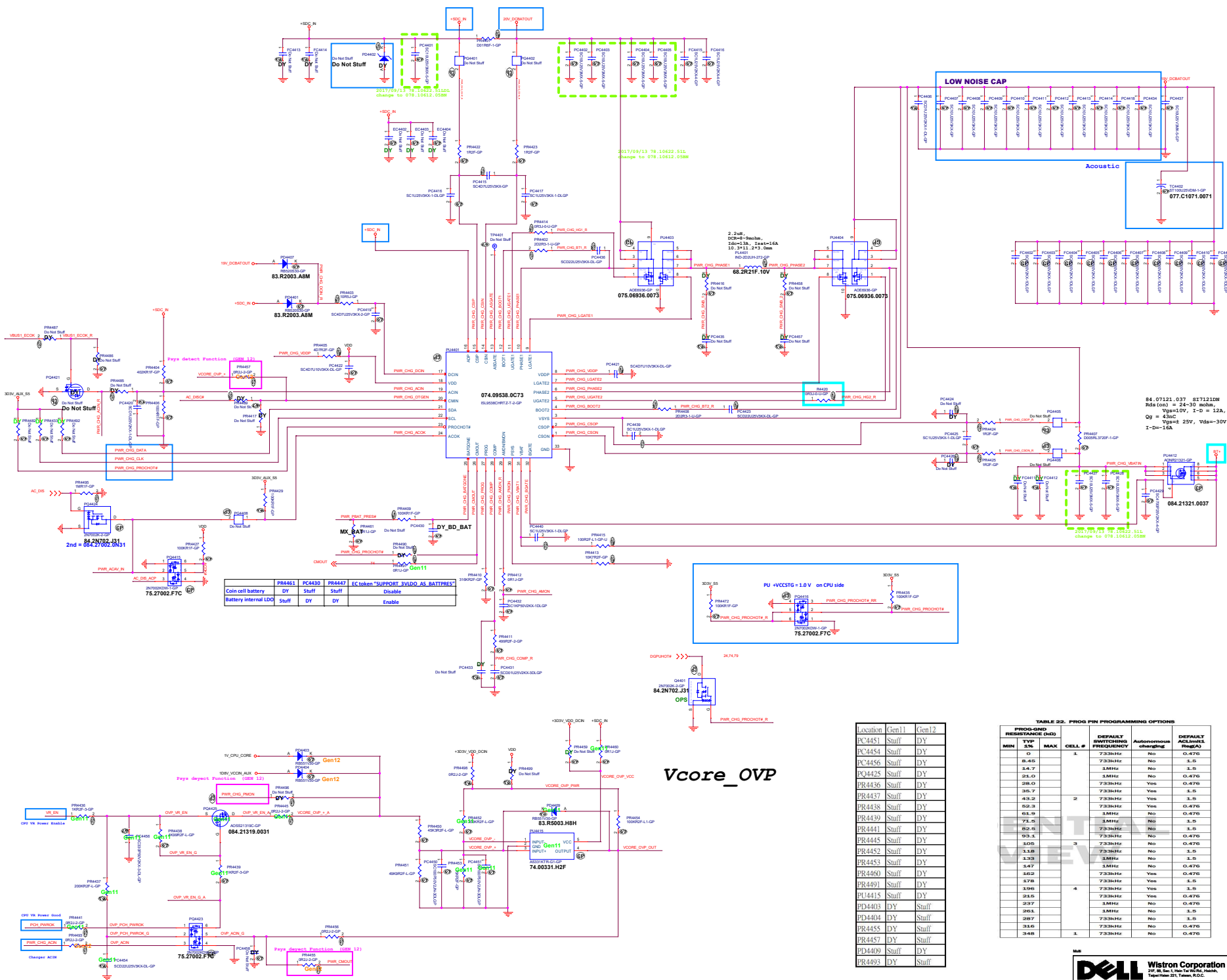
Rev

A3

SB

Date: Friday, April 24, 2020

Sheet 43 of 106

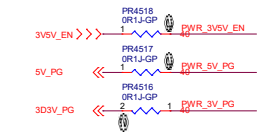


Location	Gen11	Gen12
PC4451	Staff	DY
PC4454	Staff	DY
PC4456	Staff	DY
PQ4425	Staff	DY
PR4436	Staff	DY
PR4437	Staff	DY
PR4438	Staff	DY
PR4439	Staff	DY
PR4441	Staff	DY
PR4445	Staff	DY
PR4452	Staff	DY
PR4453	Staff	DY
PR4460	Staff	DY
PR4491	Staff	DY
PJ4415	Staff	DY
PD4403	DY	Staff
PD4404	DY	Staff
PR4454	DY	Staff
PR4457	DY	Staff
PD4409	DY	Staff
PR4493	DY	Staff

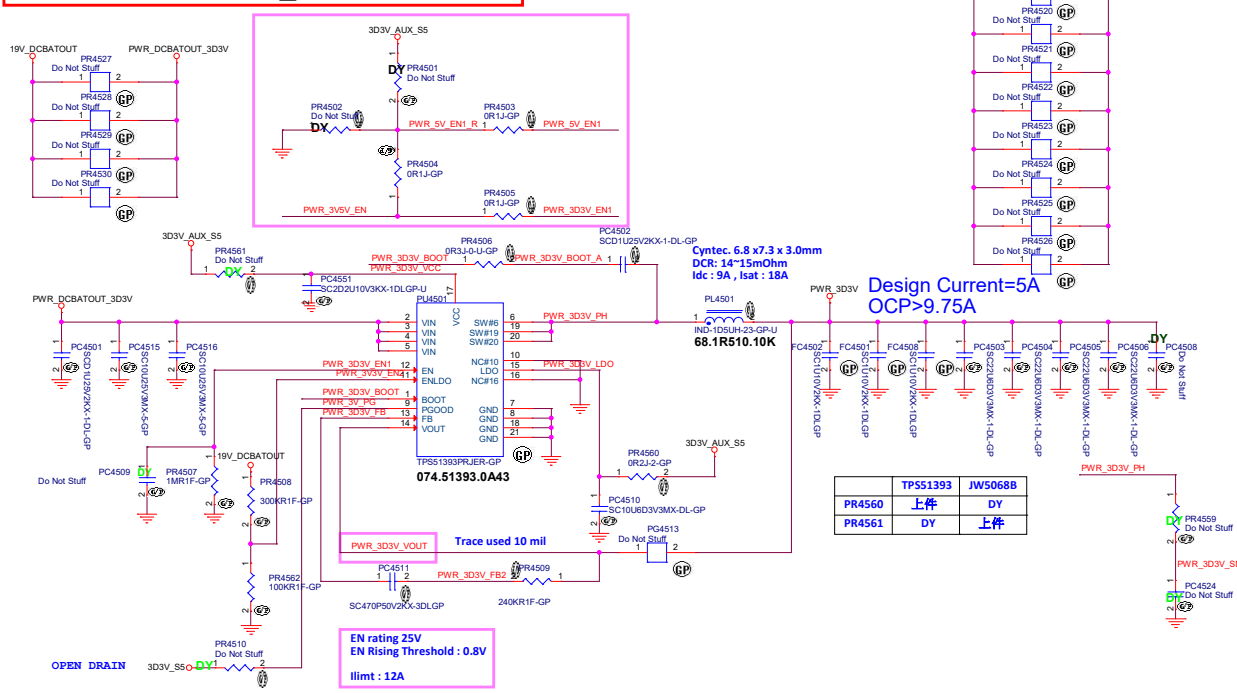
TABLE 22. PROG PIN PROGRAMMING OPTION

PROG- ID NUMBER (MS)		CELL	DEFAULT BURNING FREQUENCY	Autonomous charging	DEFAULT ACCELER Rng(A)
MIN	MAX				
8.45	1	733Hz	No	1.5	
14.7	2	1MHz	No	1.5	
25.0	3	5MHz	No	0.475	
28.0	4	733Hz	Yes	0.475	
35.7	5	733Hz	Yes	1.5	
43.3	6	733Hz	Yes	1.5	
52.0	7	733Hz	Yes	0.475	
61.9	8	5MHz	No	0.475	
71.5	9	1MHz	No	1.5	
82.0	10	733Hz	No	1.5	
93.3	11	733Hz	No	0.475	
105	12	733Hz	No	0.475	
118	13	733Hz	No	1.5	
133	14	5MHz	No	1.5	
147	15	1MHz	No	0.475	
162	16	733Hz	Yes	0.475	
178	17	733Hz	Yes	1.5	
196	18	733Hz	Yes	1.5	
215	19	733Hz	Yes	0.475	
237	20	1MHz	No	0.475	
263	21	733Hz	No	1.5	
287	22	733Hz	No	1.5	
316	23	733Hz	No	0.475	
348	24	733Hz	No	0.475	

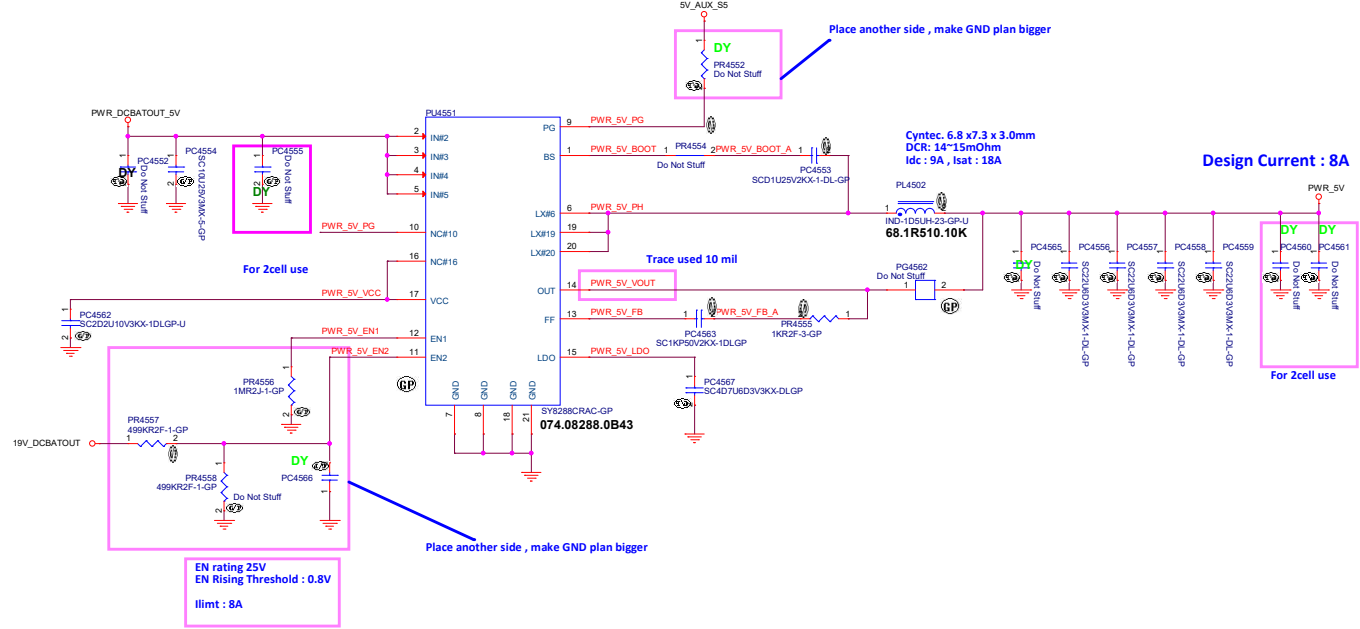
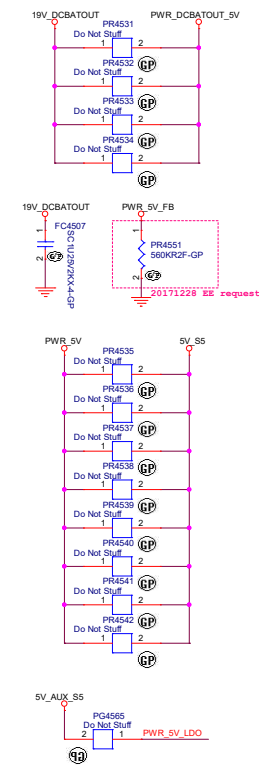
OFFPAGE

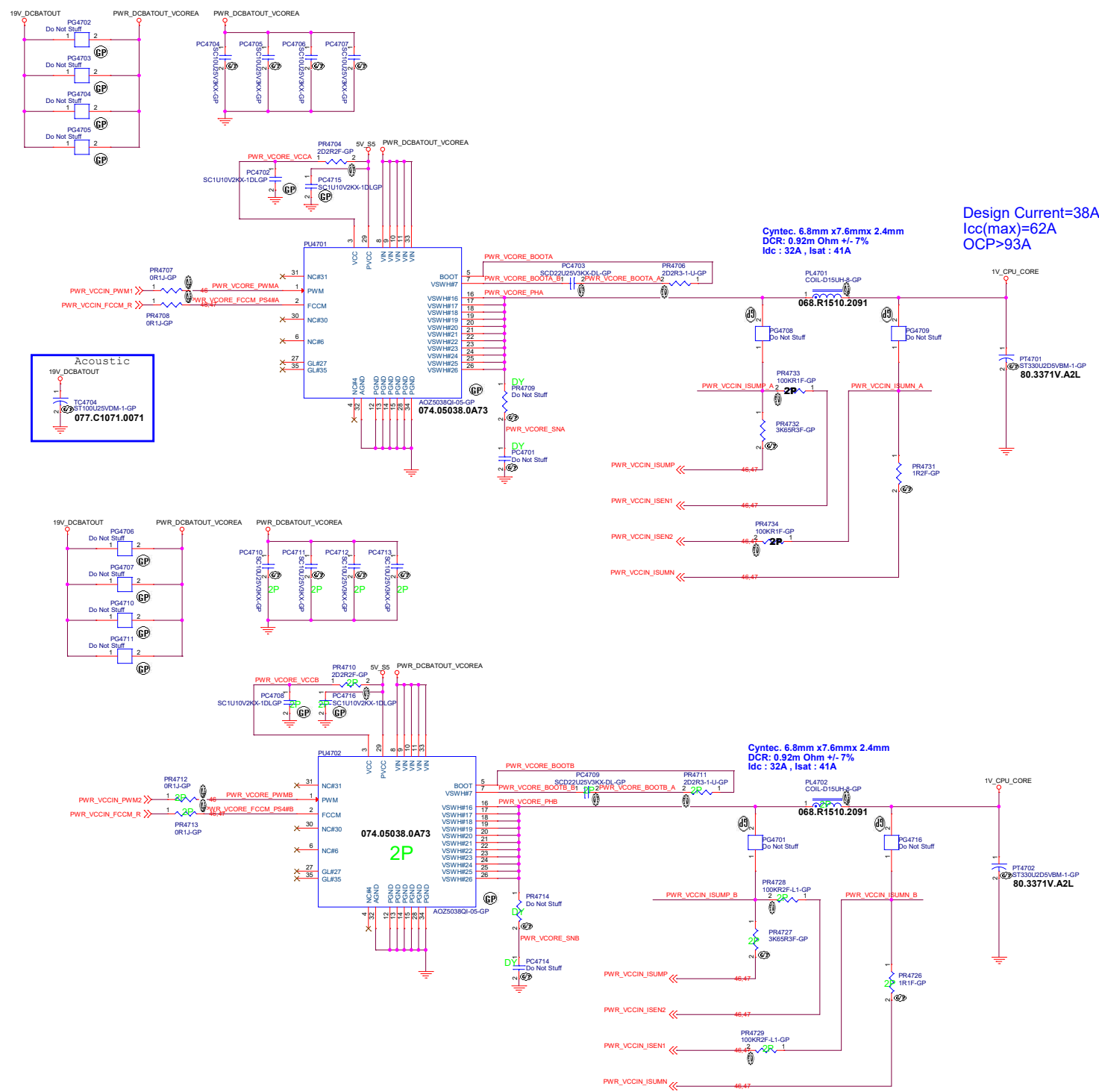


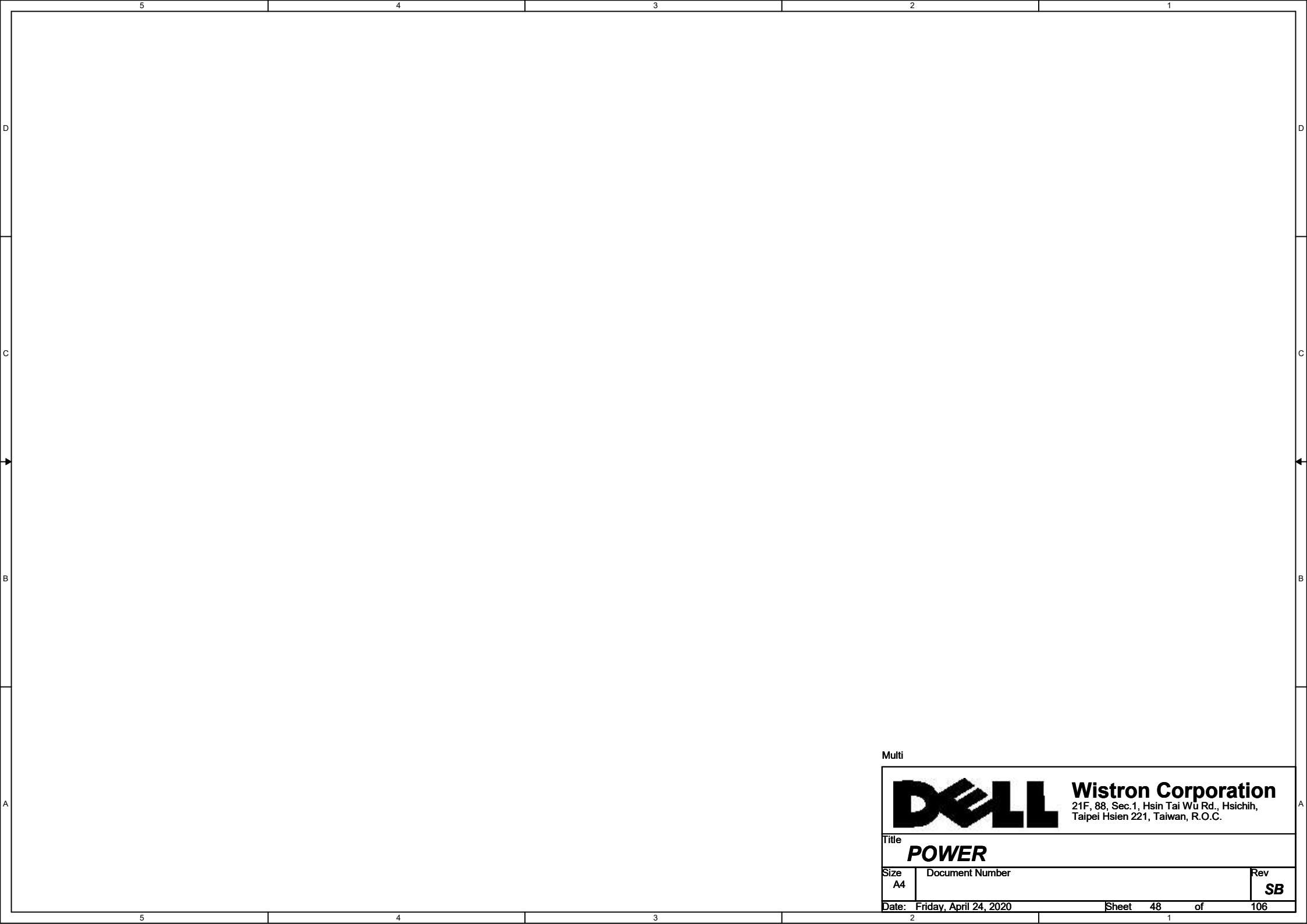
Main Func = Power_System 5V/3D3V



SY8288C For 5V







Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title POWER			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 48 of	106

5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title NCP81210MN_CPU_VCCGTUS			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 49 of	106

OFFPAGE

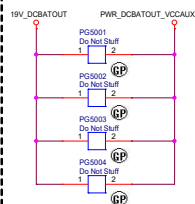
OFFPAGE GAP



PH on CPU side

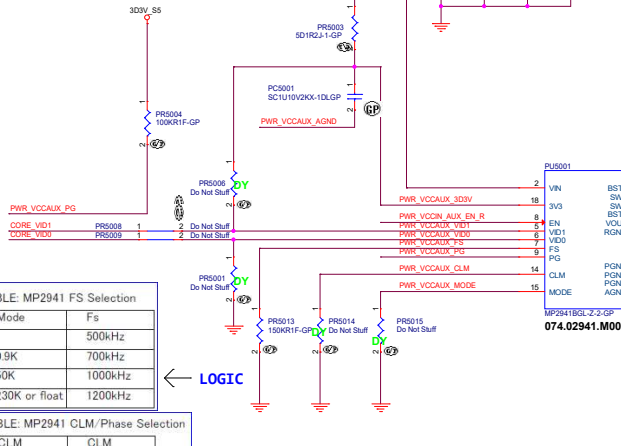


PH on CPU side



VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

LOGIC



RMode	Fs
0	500kHz
90.9K	700kHz
150K	1000kHz
>230K or float	1200kHz

LOGIC

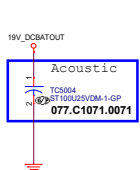
RCLM	CLM
0	7A
90.9K	10A
150K	13A
>230K or float	16A

← LOGIC

RMode	Interleaving	VID Down
0	N	Slew down
90.9K	Y	Slew down
150K	Y	Decay
>230K or float	N	Decay

← LOGIC

Item	R0 sample	R1 sample
VOUT	1.65V fixed	Defined by VCCPCHCORE_VID1/VID0
RMode	0 ohm	Float
RFS	Float	Float or 150K
1Kohm bleeder	Necessary	Not necessary

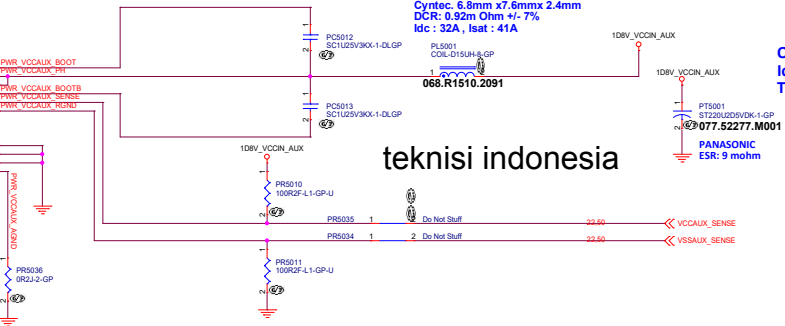


9 Pcs 22uF for 1.0MHz + 5 Pcs 22uF DY

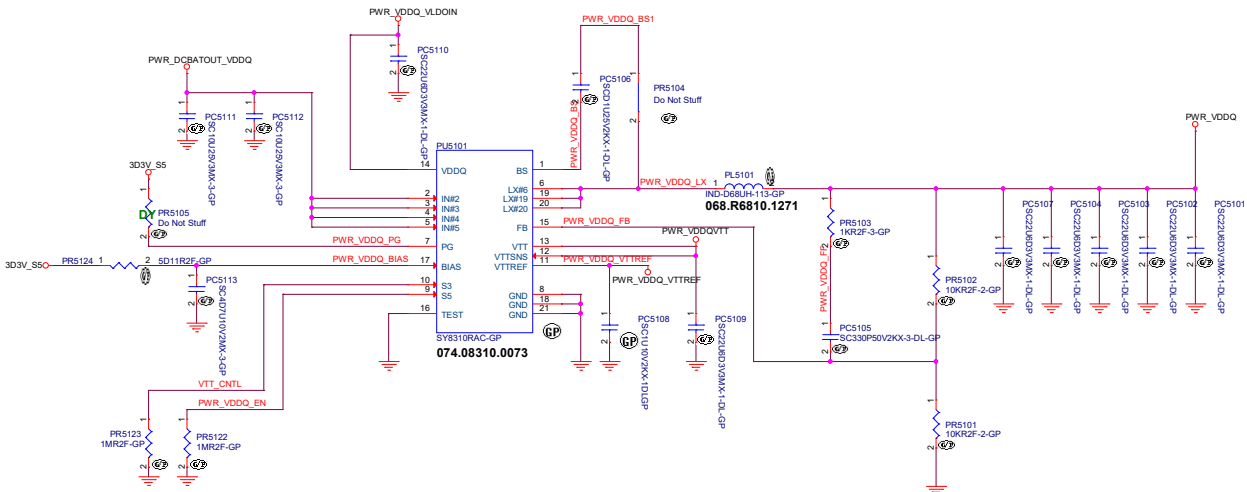
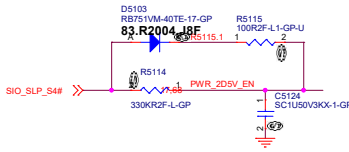
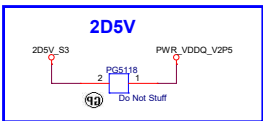
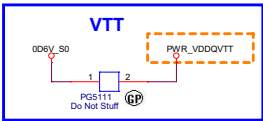
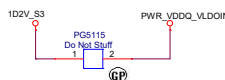
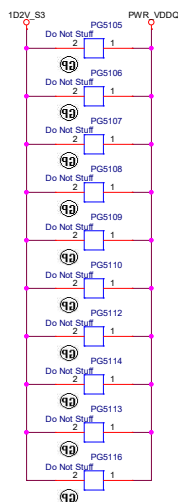
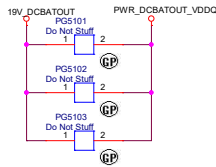
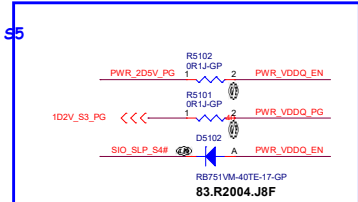
Cyntec. 6.8mm x7.6mmx 2.4mm
DCR: 0.92m Ohm +/- 7%
Idc : 32A , Isat : 41A

OCP = 40A
Iccmax= 32A
TDC=14A

teknisi indonesia



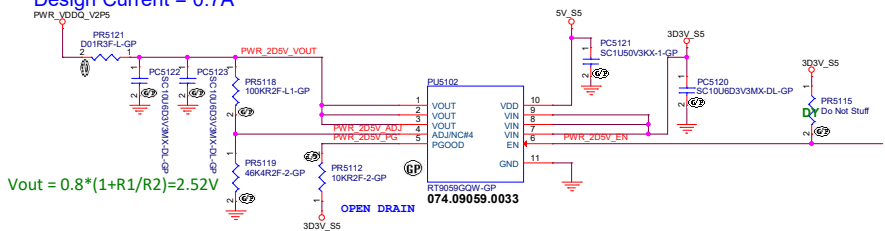
OFFPAGE GAP



MAX: 300
TPE: 210

Design Current = 0.7A

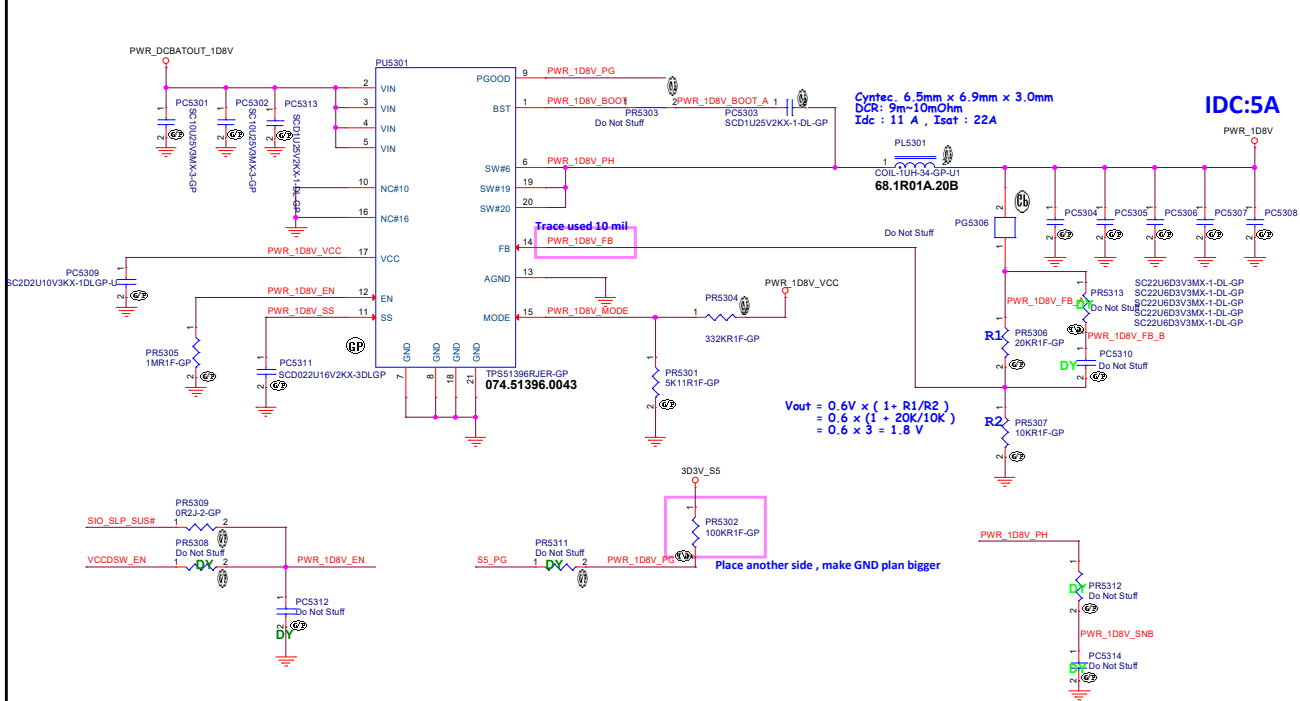
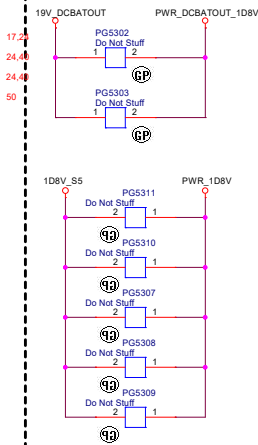
RT9059GQW for 2D5V



OFFPAGE-Signal

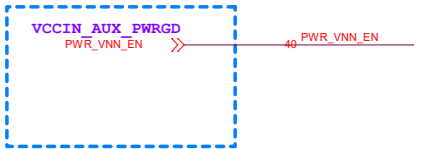
SIO_SLP_SUS# >>>
VCCDSW_EN >>>
SS_PG <<<
PWR_1D8V_PG <<<

OFFPAGE-GAP



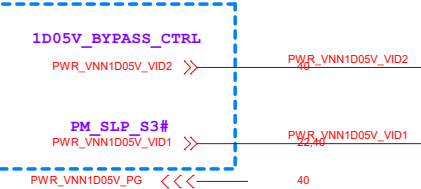
OFFPAGE

PH on EE Side

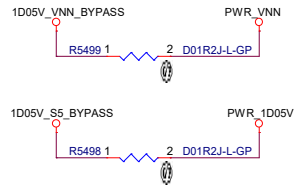


PWR_1D05V_EN >>> PWR_1D05V_EN

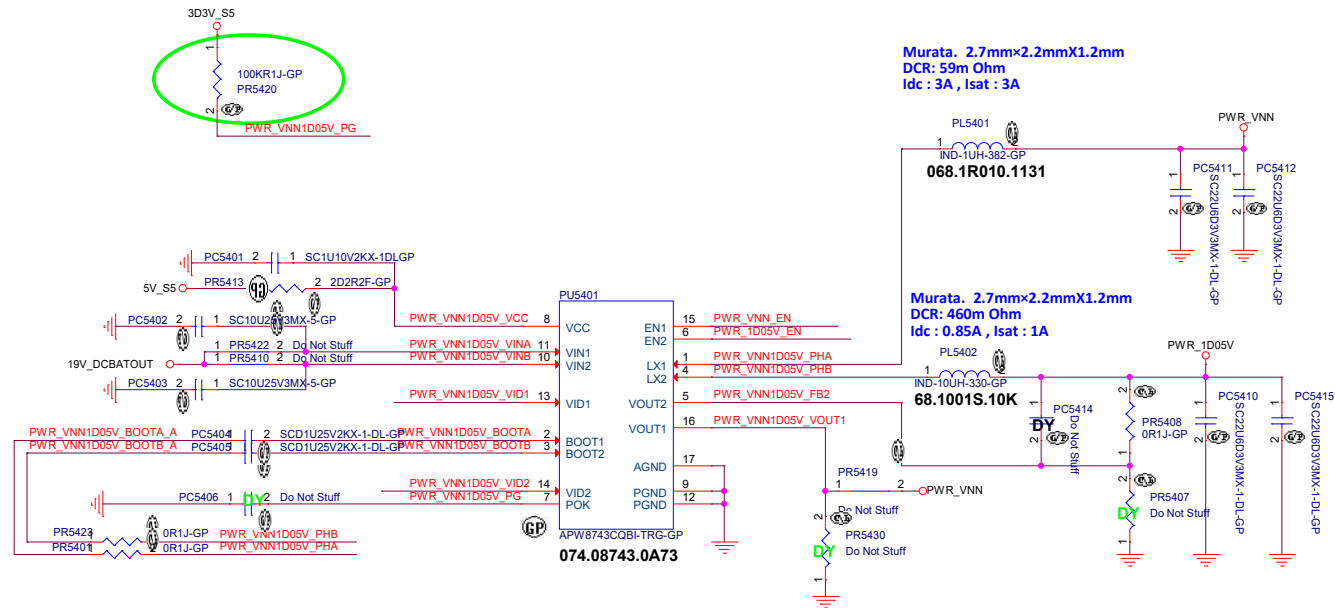
PH on EE Side



OFFPAGE-GAP



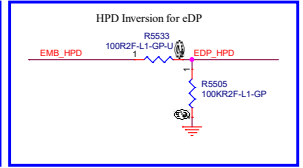
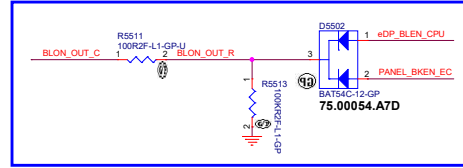
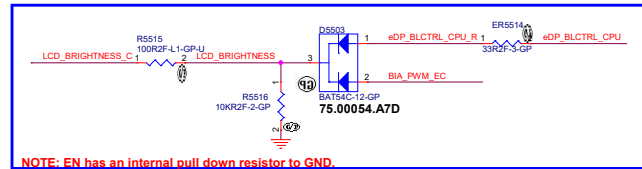
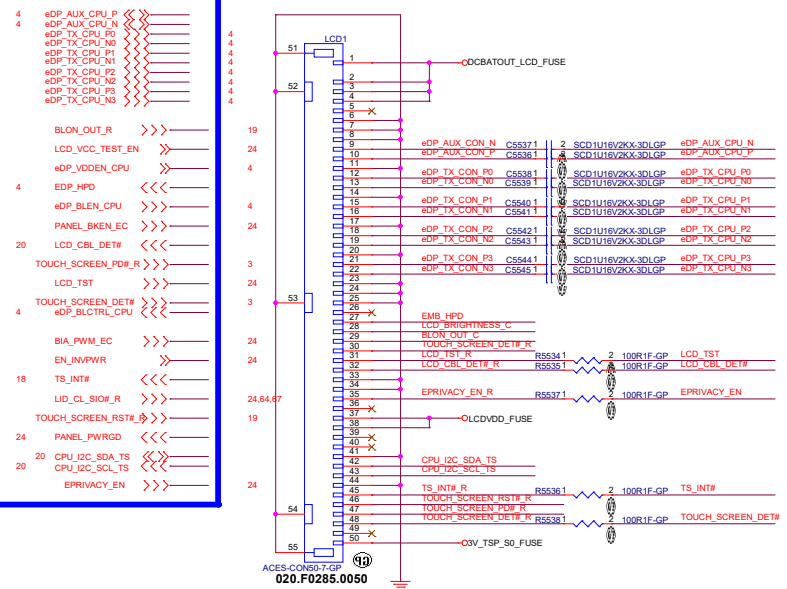
VID1 VNN OUTPUT VOLTAGE	
1	0.78 V
0	1.05 V
VID2 V1P05 OUTPUT VOLTAGE	
1	0.96 V
0	1.05 V



www.teknisi-indonesia.com

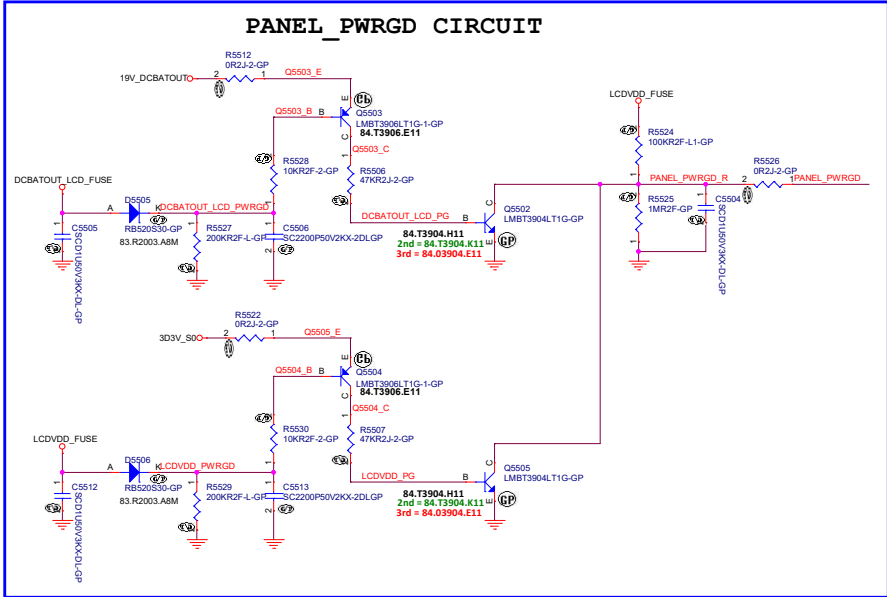
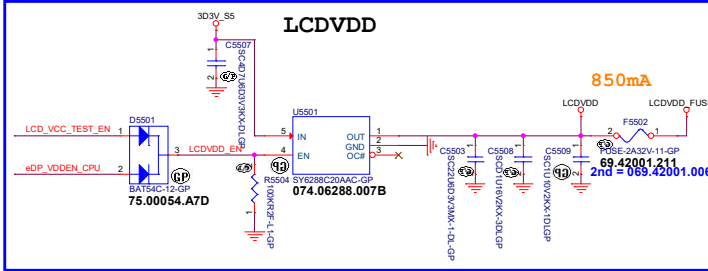
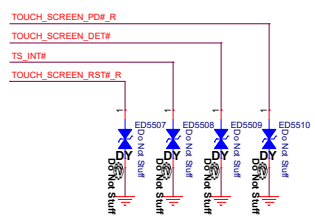
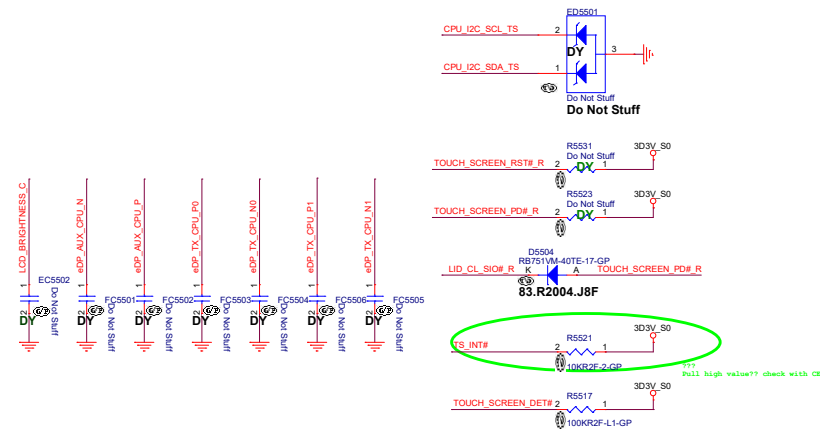
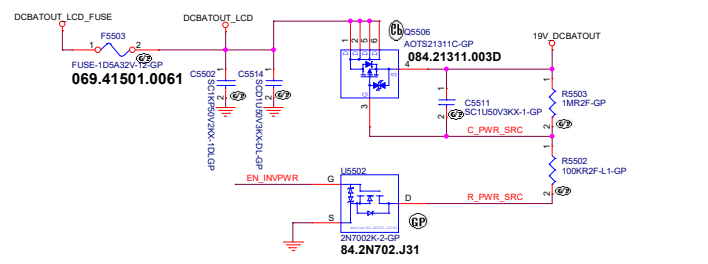
Multi			
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title APW8738_ByPASS			
Size Custom	Document Number SouthPeak15 TGL	Rev SB	
Date: Friday, April 24, 2020	Sheet 54	of	106

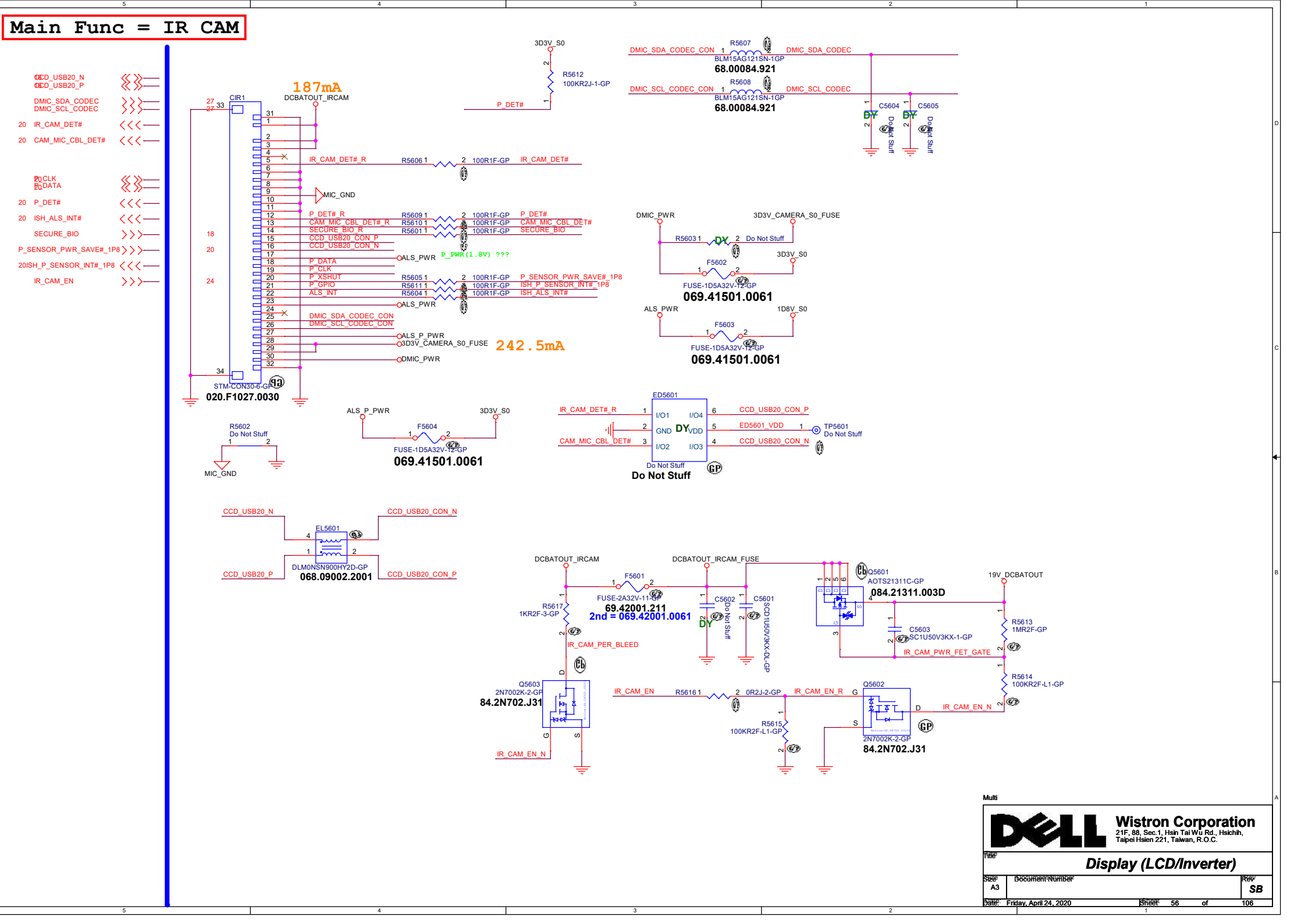
Main Func = LCD/Touch



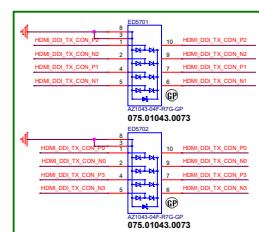
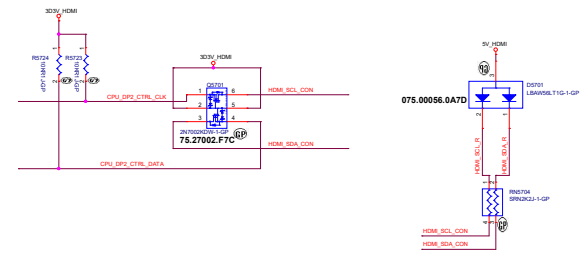
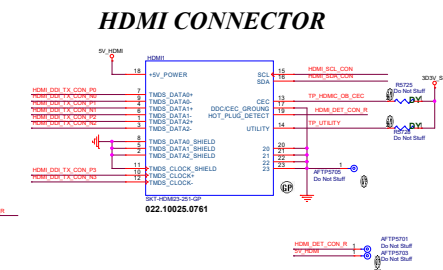
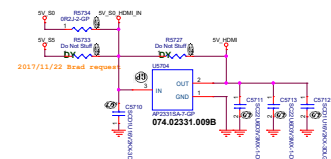
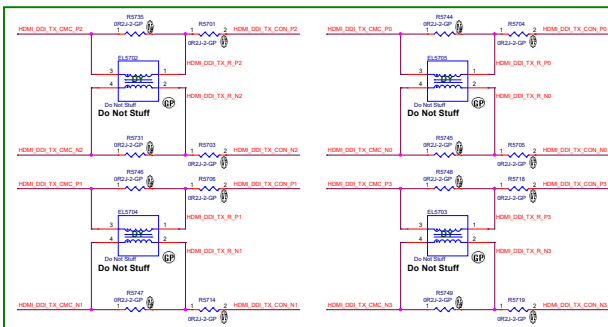
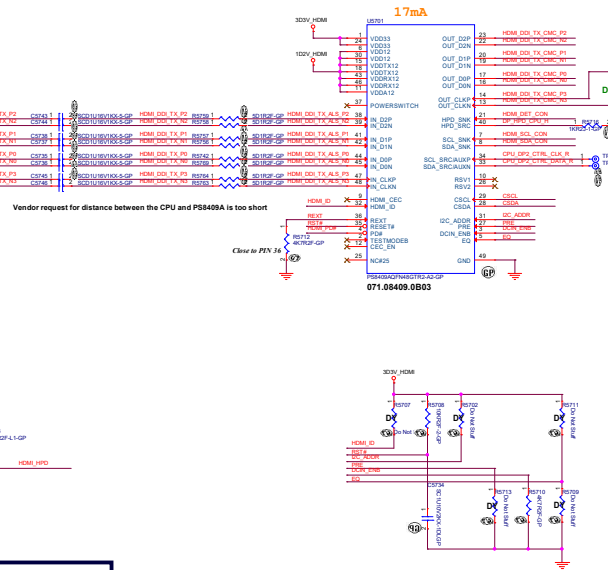
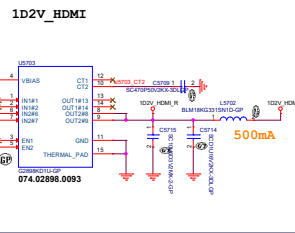
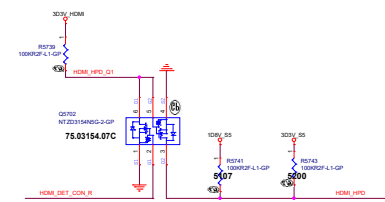
1086mA

INVERTER POWER



[illegible]

	RUN_ON_R	>>>	
	DP2_DDI_TX_P0	>>>	
	DP2_DDI_TX_N0	>>>	
	DP2_DDI_TX_P1	>>>	
	DP2_DDI_TX_N1	>>>	
	DP2_DDI_TX_P2	>>>	
	DP2_DDI_TX_N2	>>>	
	DP2_DDI_TX_P3	>>>	
	DP2_DDI_TX_N3	>>>	
	HDMI_P0W	>>>	
4	DP_HPD_CPU	<<<	
4	CPU_DP2_CTLB_CLK	<<<	
4	CPU_DP2_CTLB_DATA	<<<	
24	CISCL	<<<	
24	CISDA	<<<	
24	HDMI_HPD	<<<	



www.teknisi-indonesia.com

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Display (RSVD) DP			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 58 of	106

5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

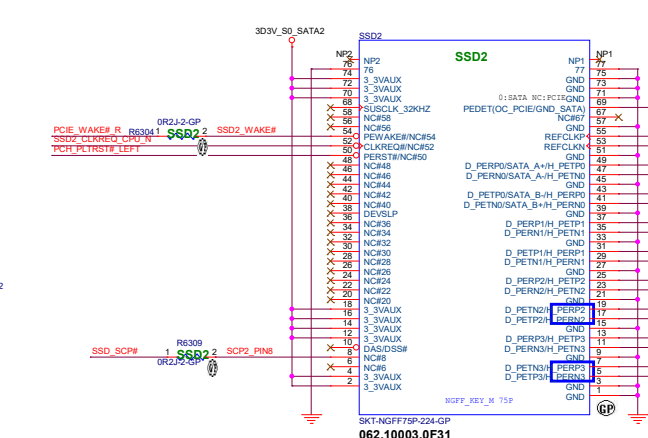
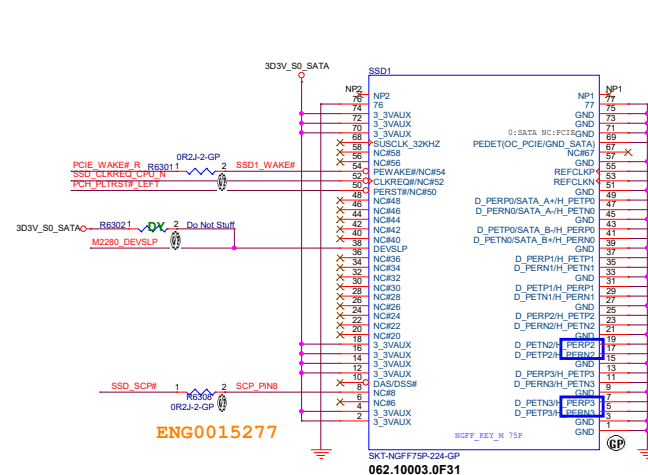
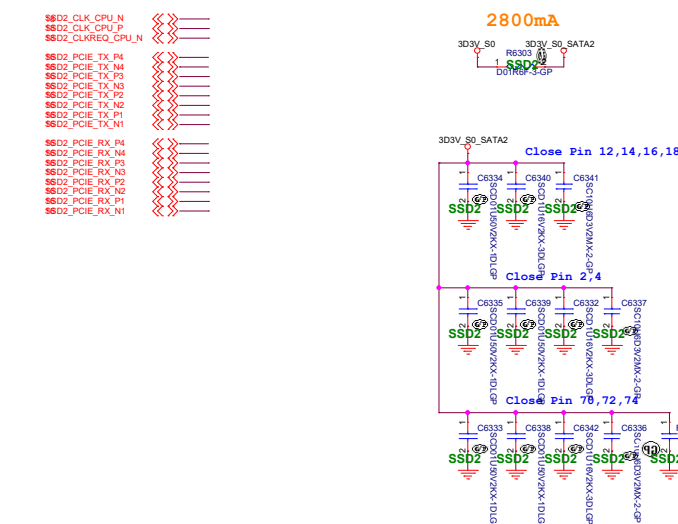
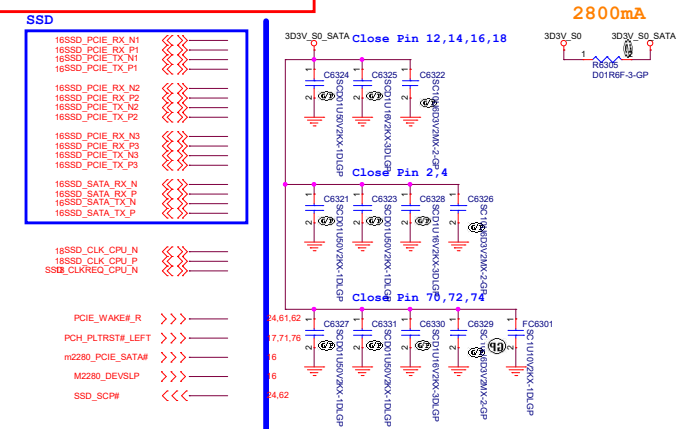
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Display (RSVD) DVI			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 59 of	106

5	4	3	2	1
D				
C				
B				
A				

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title INT IO (RSVD)(HDD)			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 60 of	106

Main Func = m.2 SSD



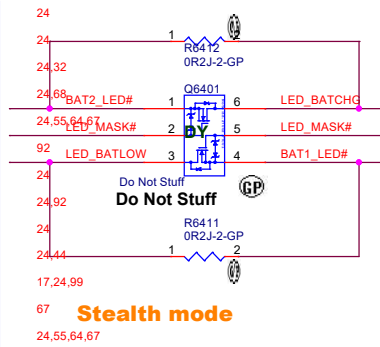
PEDET	0	Host I/F Indication; To be grounded for SATA, No Connect for PCIe	OVNI
-------	---	--	------

L	SATA
H	PCI-E

74	3.3V	GN2	75
72	3.3V	GN2	73
70	3.3V	GN2	71
68	SUSCLK(32MHz) (I/O[3..3V])	PEDET (NC-PeDet/GND-SATA)	69
	Connector Key	N/C	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	GN2	57
56	N/C	REFCLKP	55
54	PEWAKE (I/O[10..3..3V]) or N/C	REFCLKN	53
52	CLKREQ (I/O[10..3..3V]) or N/C	GN2	51
50	PERST (I/O[3..3V]) or N/C	PETP0/SATA-A+	49
48	N/C	PETP0/SATA-A-	47
46	N/C	GN2	45
44	N/C	PERP0/SATA-B-	43
42	N/C	PERP0/SATA-B+	41
40	N/C	GN2	39
38	DEVSLP (O)	PETP1	37
36	N/C	PETP1	35
34	N/C	GN2	33
32	N/C	PERP1	31
30	N/C	PERP1	29
28	N/C	GN2	27
26	N/C	PETP2	25
24	N/C	PETP2	23
22	N/C	GN2	21
20	N/C	PERP2	19
18	N/C	PERP2	17
16	3.3V	GN2	15
14	3.3V	PETP3	13
12	3.3V	PETP3	11
10	DA5/D5# (I/O)/LED5# (I/O[3..3V])	GN2	9
8	N/C	PERP3	7
6	N/C	PERP3	5
4	N/C	GN2	3
2	3.3V	GN2	1

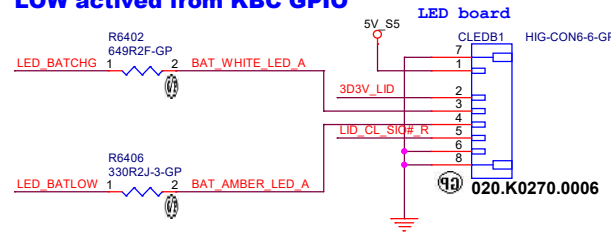
Main Func = LED/HALL/Button

BAT2_LED# >>>
 BAT1_LED# >>>
 LED_MASK# >>>
 KBC_PWRBTN# <<<
 LID_CL_SIO#_R <<<
 MASK_BASE_LEDS#_Q <<<
 BREATH_LED# <<<
 FPR_DET# >>>
 M_BIST >>>
 ACAV_IN >>>
 RSMRST#_KBC >>>
 3D3V_LID >>>
 LID_CL_SIO#_R >>>

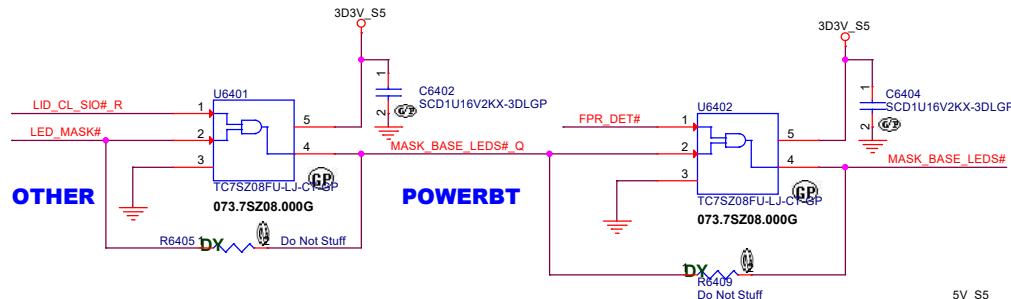
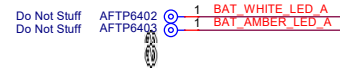


Stealth mode

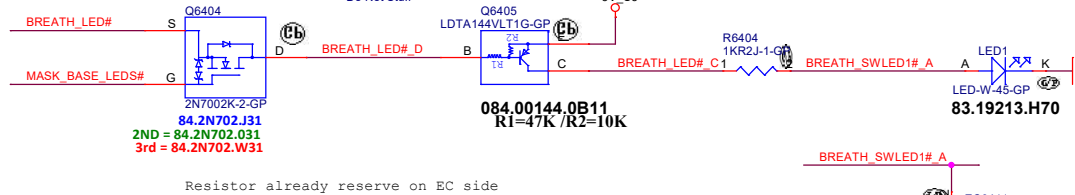
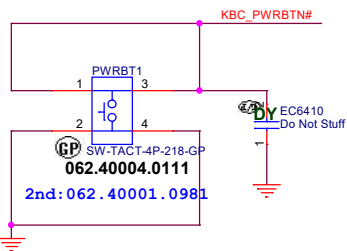
Battery LED2(White LED) LOW acted from KBC GPIO



Battery LED1(Orange LED) LOW acted from KBC GPIO



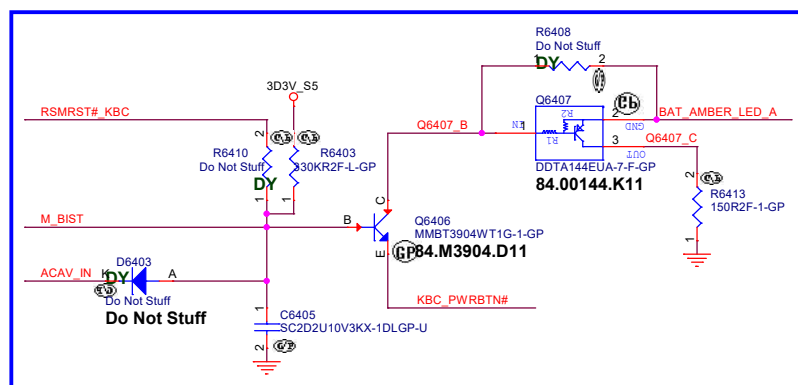
POWER BUTTON



Resistor already reserve on EC side

Power LED LOW acted from KBC GPIO

M-BIST



Multi

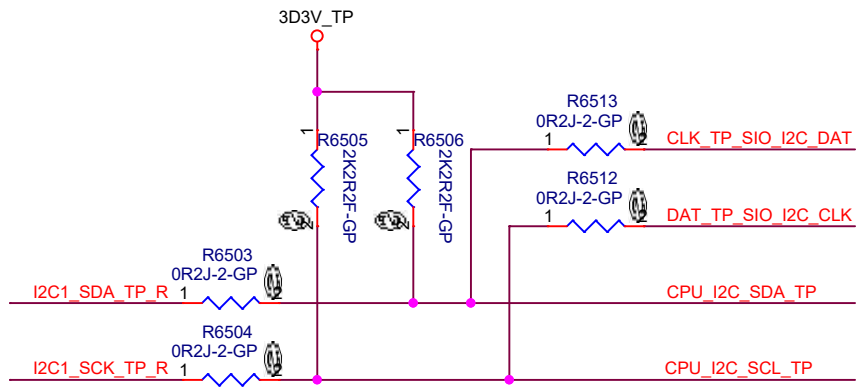
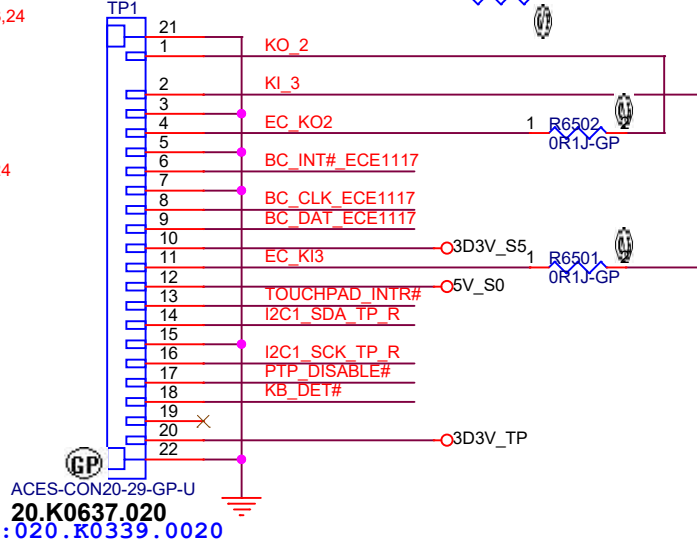
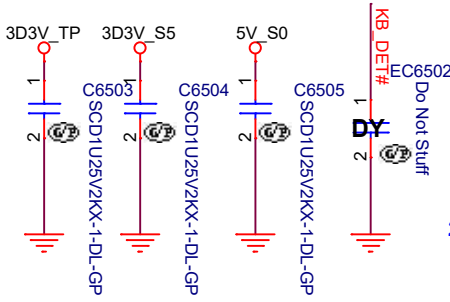
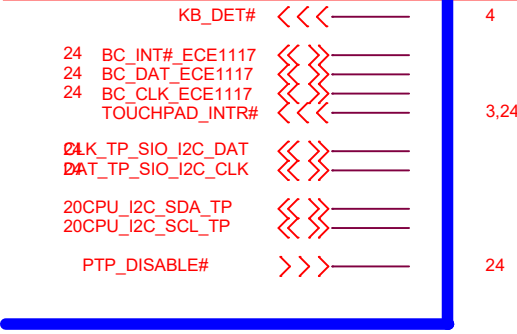
DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
 Taipei Hsien 221, Taiwan, R.O.C.

FILE **LED / Button / Power Button**

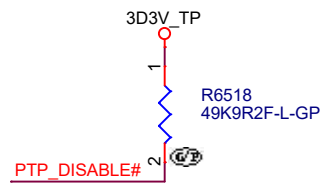
Size Custom Document Number Rev SB

Date: Friday, April 24, 2020 Sheet 64 of 106

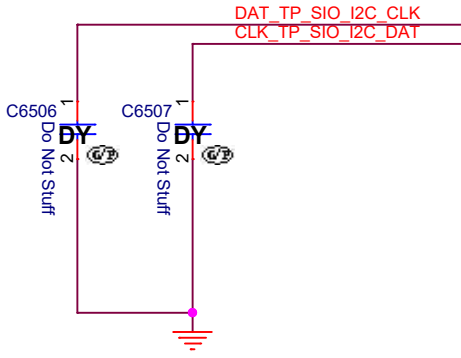
Main Func = Key Board/Touch Pad



10mA



www.teknisi-indonesia.com

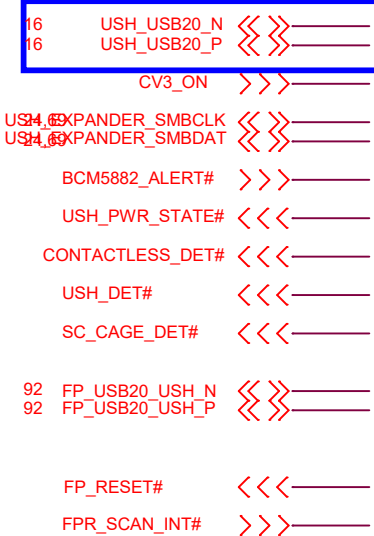


Multi

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title INT IO (KB/TP)			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020	Sheet 65 of		106

Main Func = USH BD

USH



CV3 module	
pin assignment -proposal 2	
NC	
NC	
CV2_ON	
USB20_N from FPR	
USB20_P from FPR	
GND	
GND	
USB20_N to PCH	
USB20_P to PCH	
GND	
USH_EXPANDER_SMBCLK	
USH_EXPANDER_SMBDAT	
BCM5882_ALERT#	
+3.3V_ALW	
+3.3V_ALW	
+3.3V_ALW	
+3.3V_ALW	
+3.3V_RUN	
+3.3V_RUN	
USH_RST#	
USH_PWR_STATE#	
CONTACTLESS_DET#	
GND	
GND	
USH_DET#	

SC_CAGE_DET#

FP_RESET#

CV3_ON

FP_USB20_USH_N

FP_USB20_USH_P

USH_USB20_CON_N

USH_USB20_CON_P

USH_EXPANDER_SMBCLK

USH_EXPANDER_SMBDAT

BCM5882_ALERT#

3D3V_S5

5V_S5

3D3V_S0

5V_S0

FPR_SCAN_INT#

USH_PWR_STATE#

CONTACTLESS_DET# USH

D6602
RB751VM-40TE-17-GP

83.R2004.J8F

92 CONTACTLESS_DET#

24,92

USH_DET#

R6607
0R2J-2-GP

D6601

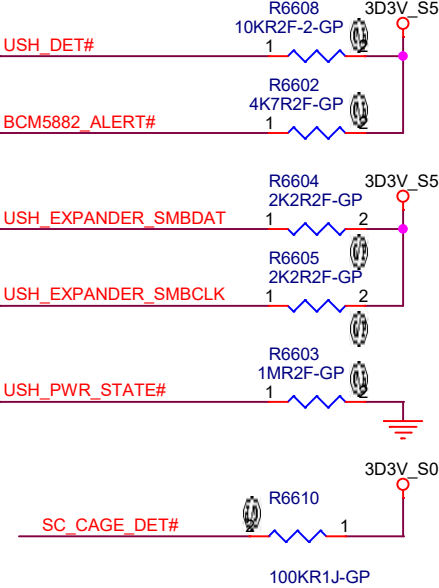
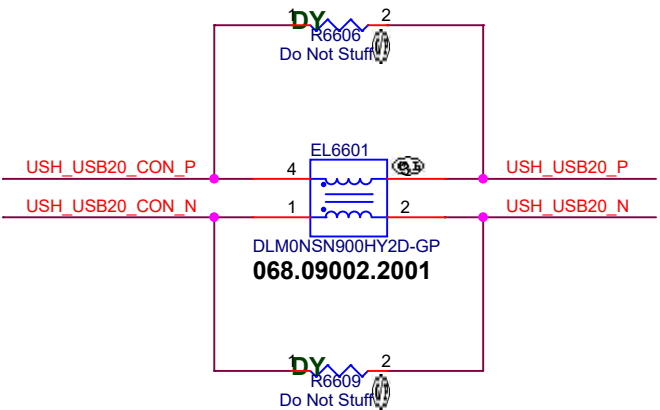
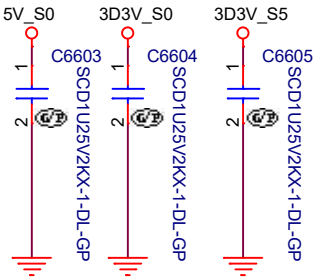
Do Not Stuff

Do Not Stuff

USH_DET#_R

ACES-CON26-17-GP-U1

20.K0637.026

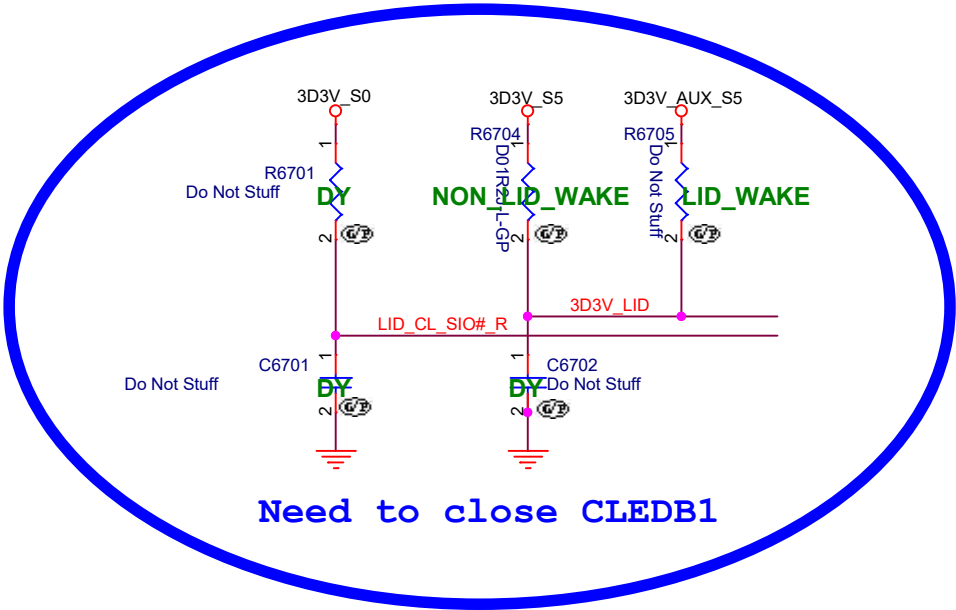


Multi

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title IO Board Conn (USH)			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 66	of 106

Main Func = Sensor (Hall-Sensor)

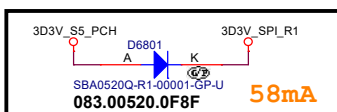
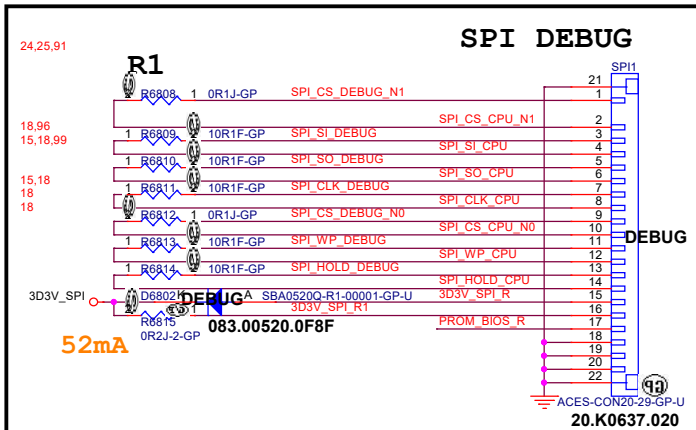
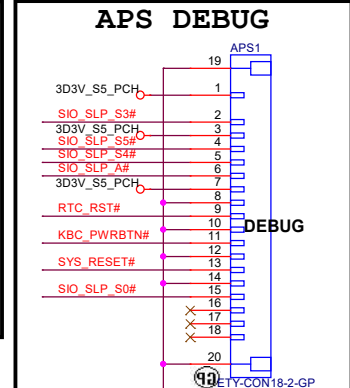
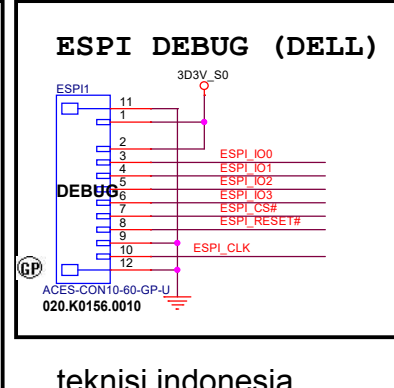
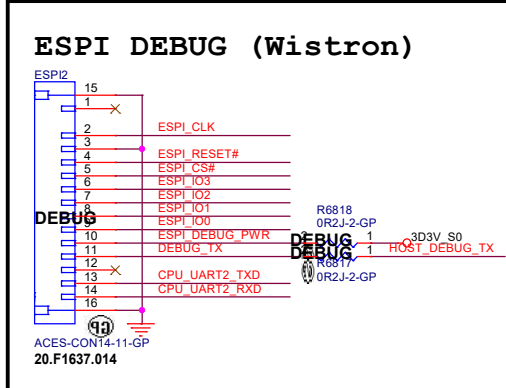
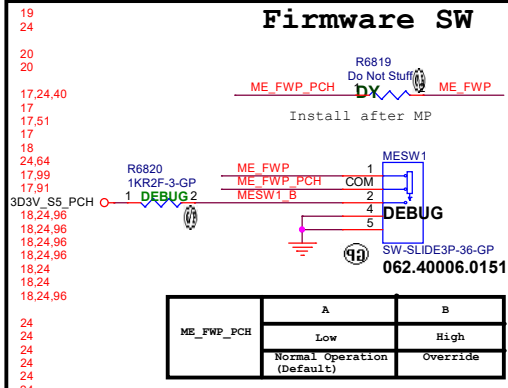
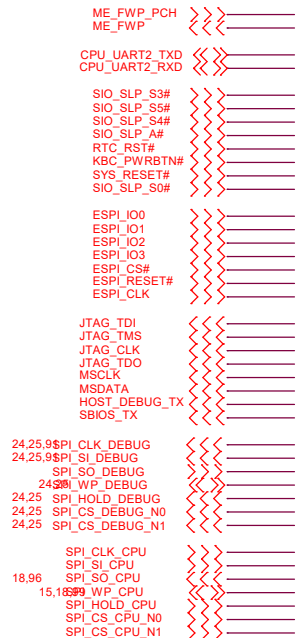
24,53,63 CL_SIO#_R << >>—
3D3V_LID <<<— 64



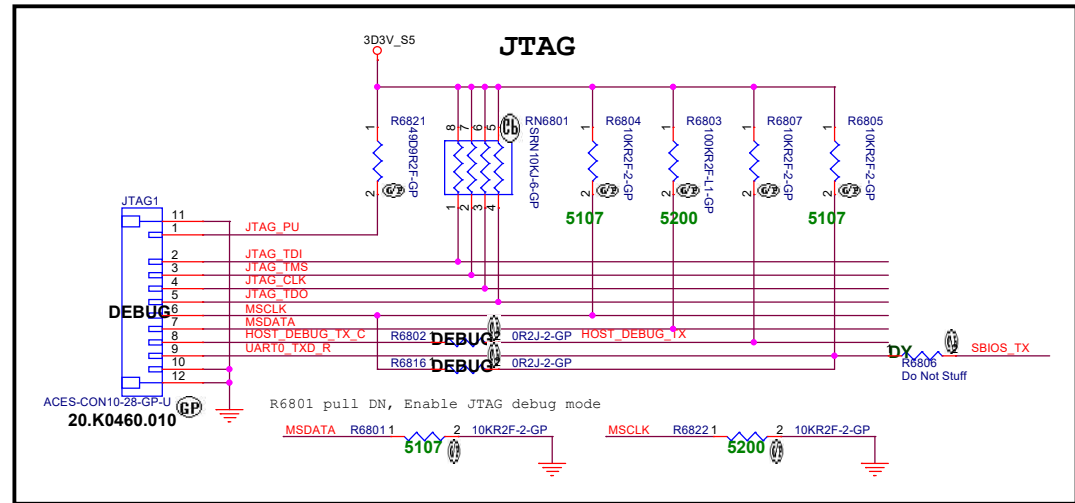
Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Sensor (Hall-Sensor)			
Size A4	Document Number		Rev SB
Date:	Friday, April 24, 2020	Sheet	67 of 106

Main Func = Debug

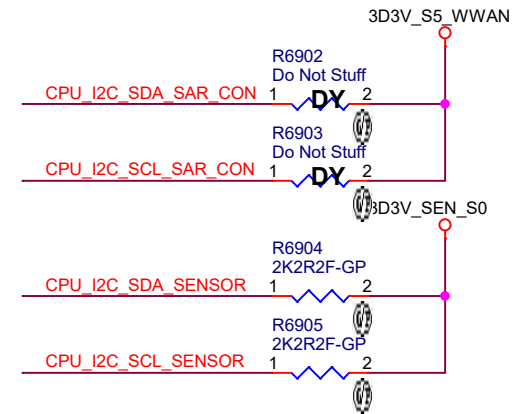
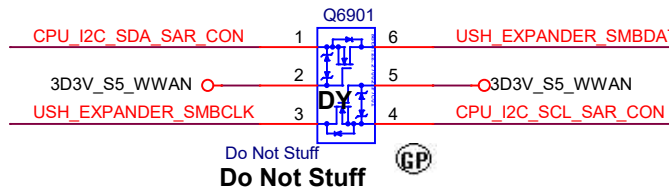
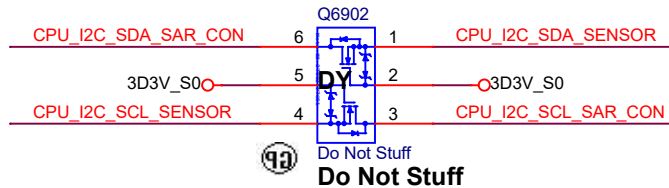
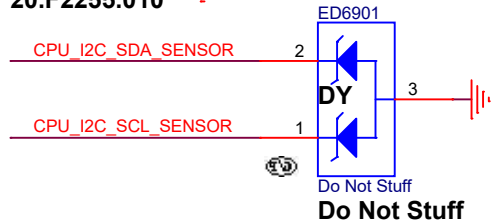
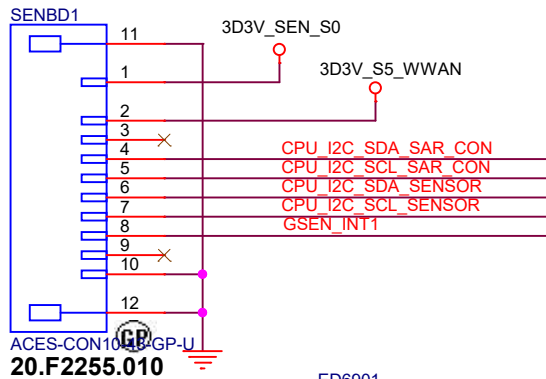
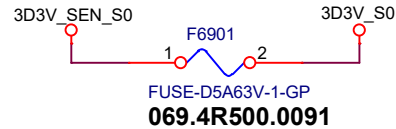


MP change to short pad



Main Func = Sensor (E-compass/A+Gyro/SAR)

20 GSEN_INT1 <<< ———
CPU_I2C_SCL_SENSOR <<< ———
CPU_I2C_SDA_SENSOR <<< ———
USH_EXPANDER_SMBDAT <<< ———
USH_EXPANDER_SMBCLK <<< ———

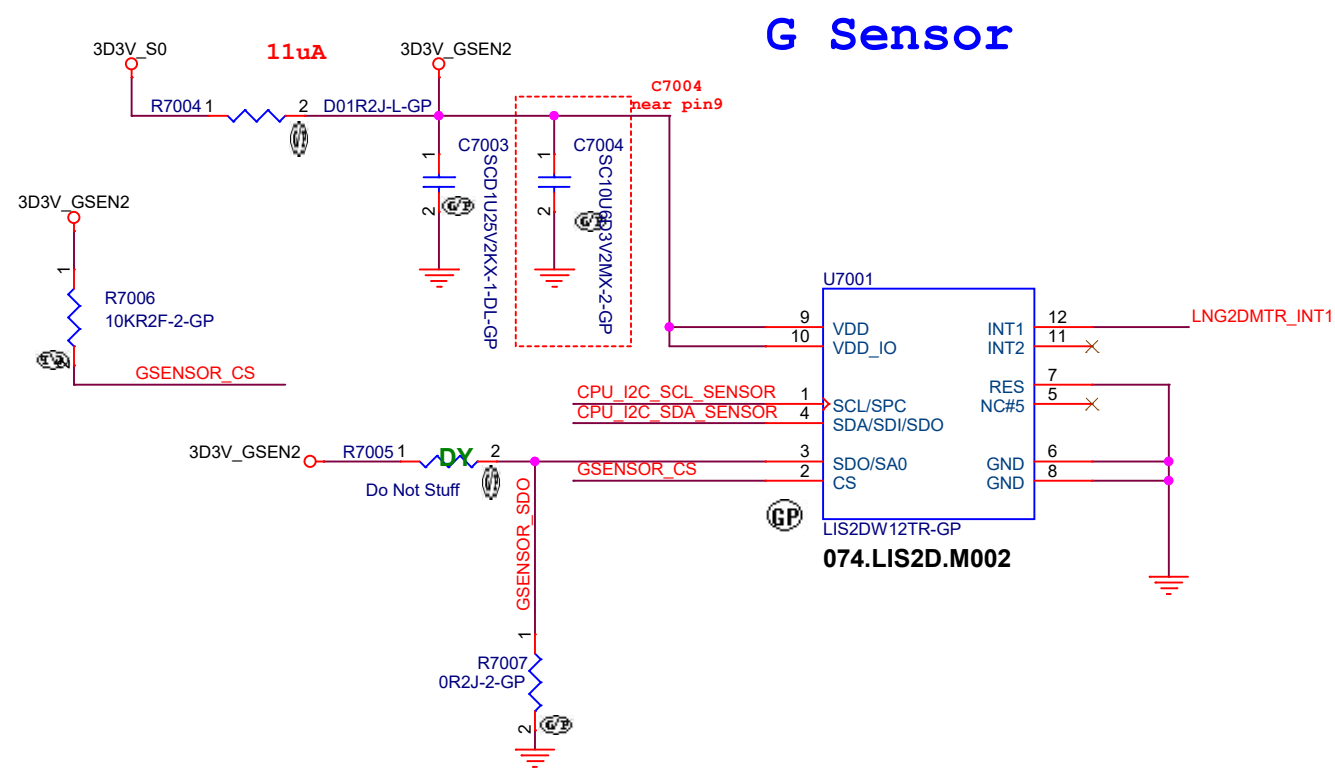


Multi

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Sensor (GYROSCOPE/PRESSUE/ALS)			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020	Sheet 69 of 106		

Main Func = G-sensor

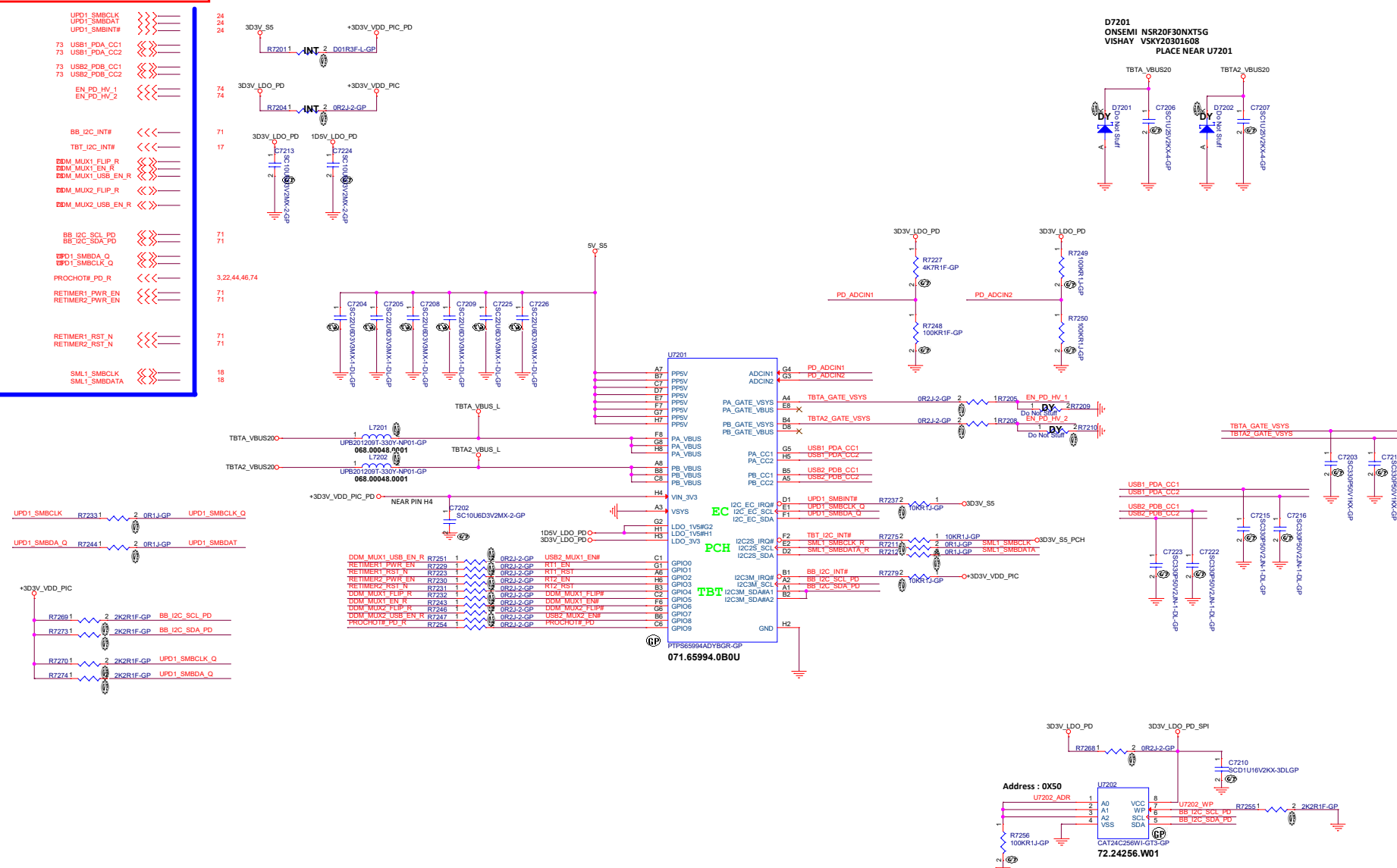
0P60 I2C_SDA_SENSOR
0P60 I2C_SCL_SENSOR
20 LNG2DMTR_INT1



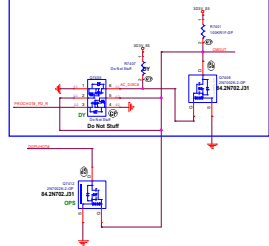
Multi

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Sensor (G-sensor)			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 70	of 106

Main Func = TypeC



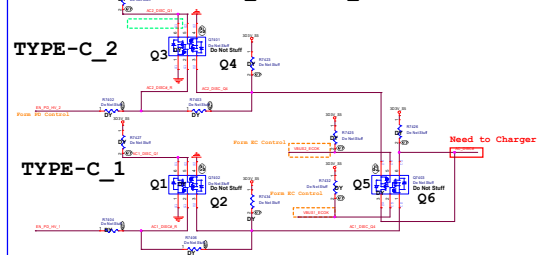
AC Disconnect Latch



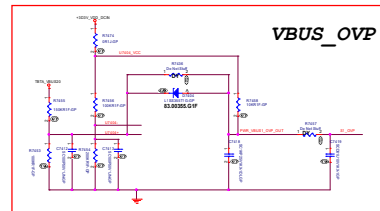
AC_Disconnect_Logic

TYPE-C_2

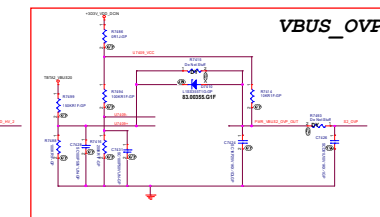
TYPE-C_1



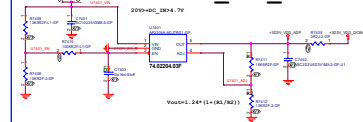
VBUS_OVP



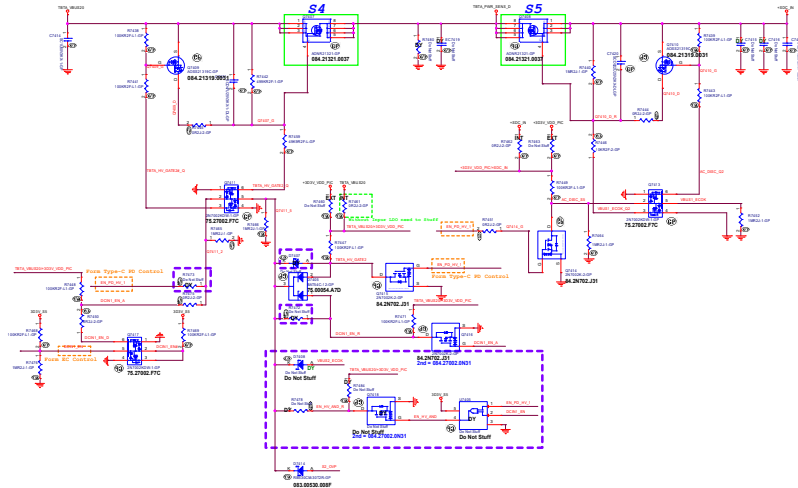
VBUS_OVP



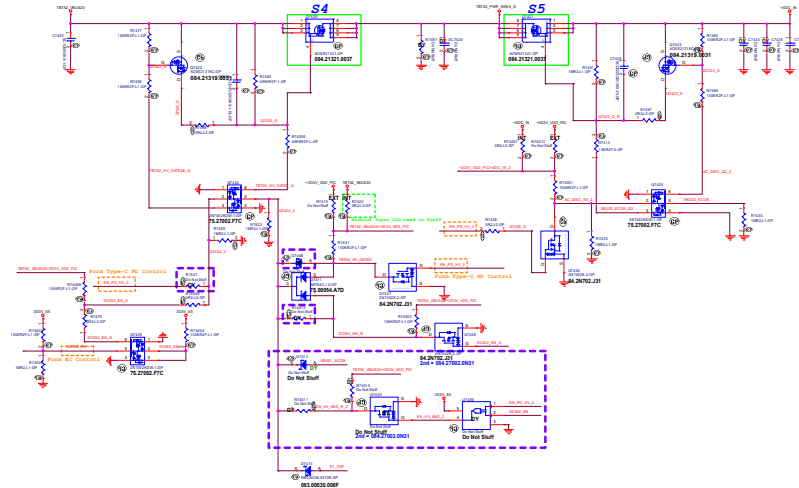
+3D3V_VDD_DCIN



TYPE-C 1



TYPE-C 2

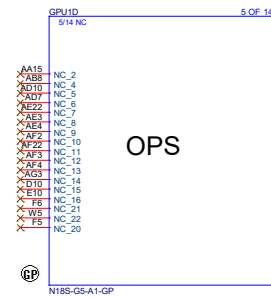
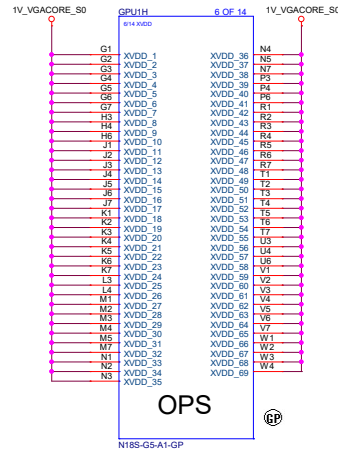
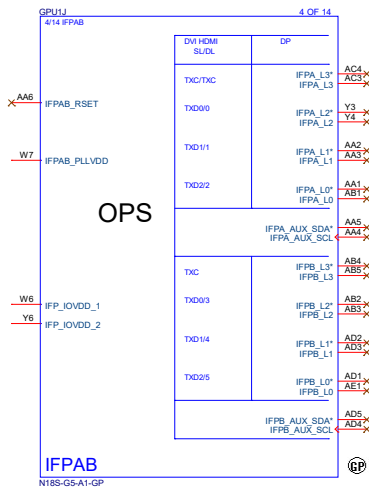


5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title EXT IO (RSVD)			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 75 of	106

Main Func = dGPU



Mult

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichang,
Taipei Hsien 221, Taiwan, R.O.C.

File: GPU DIGITALOUT (2/5)

Size A2 Document Number: SouthPeak15 TGL Rev: SB

Date: Friday, April 24, 2020 Sheet 77 of 106

Main Func = GPU	
1	GPU_VDD1
2	GPU_VDD2
3	GPU_VDD3
4	GPU_VDD4
5	GPU_VDD5
6	GPU_VDD6
7	GPU_VDD7
8	GPU_VDD8
9	GPU_VDD9
10	GPU_VDD10
11	GPU_VDD11
12	GPU_VDD12
13	GPU_VDD13
14	GPU_VDD14
15	GPU_VDD15
16	GPU_VDD16
17	GPU_VDD17
18	GPU_VDD18
19	GPU_VDD19
20	GPU_VDD20
21	GPU_VDD21
22	GPU_VDD22
23	GPU_VDD23
24	GPU_VDD24
25	GPU_VDD25
26	GPU_VDD26
27	GPU_VDD27
28	GPU_VDD28
29	GPU_VDD29
30	GPU_VDD30
31	GPU_VDD31
32	GPU_VDD32
33	GPU_VDD33
34	GPU_VDD34
35	GPU_VDD35
36	GPU_VDD36
37	GPU_VDD37
38	GPU_VDD38
39	GPU_VDD39
40	GPU_VDD40
41	GPU_VDD41
42	GPU_VDD42
43	GPU_VDD43
44	GPU_VDD44
45	GPU_VDD45
46	GPU_VDD46
47	GPU_VDD47
48	GPU_VDD48
49	GPU_VDD49
50	GPU_VDD50

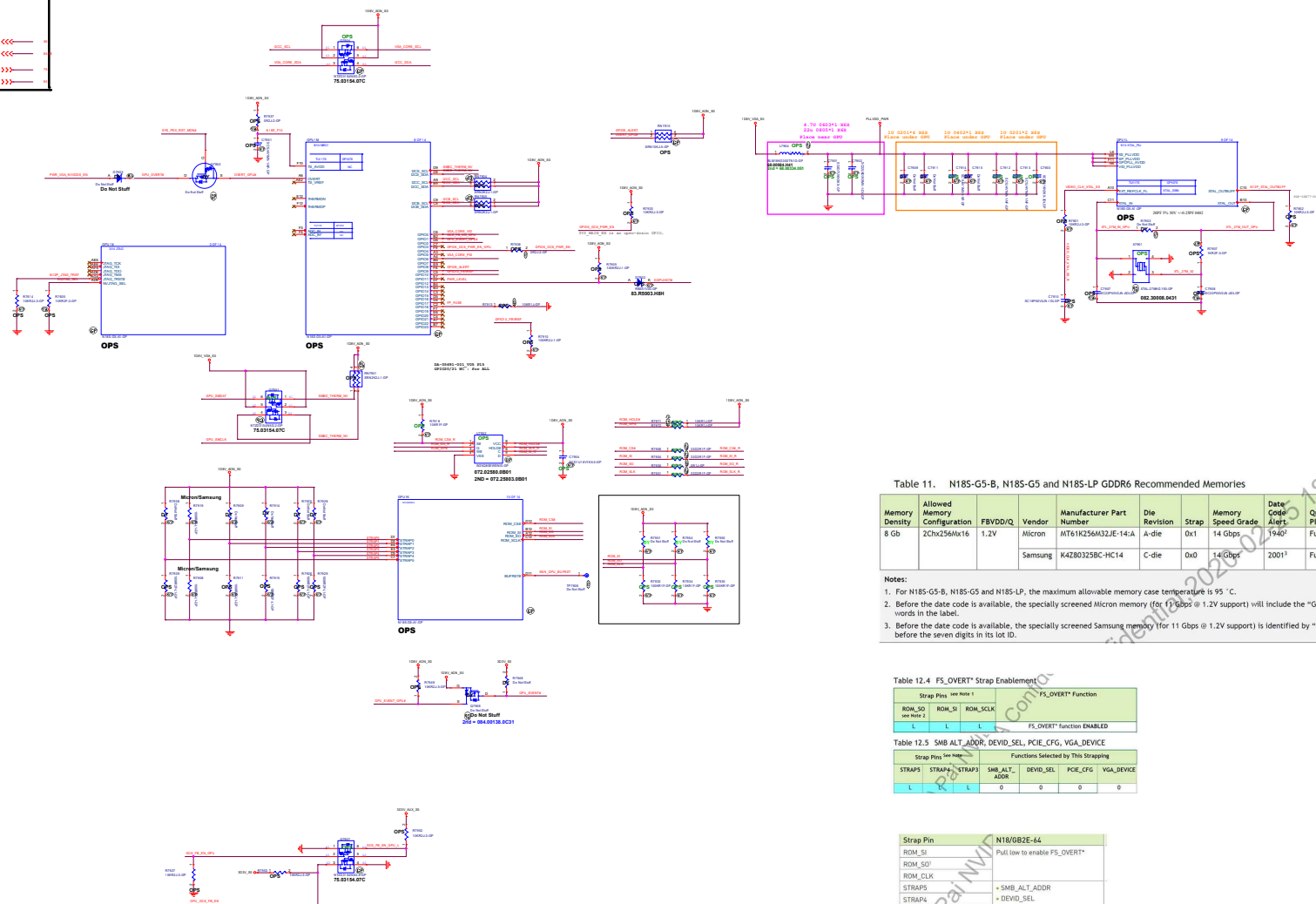


Table 11. N185-G5-B, N185-G5 and N185-LP GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Nx16	1.2V	Micron	MT61K256M32JE-14-A	A-die	0x1	14 Gbps	1940 ²	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001 ³	Full	Production candidate

Notes:

- For N185-G5-B, N185-G5 and N185-LP, the maximum allowable memory case temperature is 95 °C.
- Before the date code is available, the specially screened Micron memory (for 11 Gbps @ 1.2V support) will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
- Before the date code is available, the specially screened Samsung memory (for 11 Gbps @ 1.2V support) is identified by "SPL" letters inserted before the seven digits in its lot ID.

Table 12.4 FS_OVERT* Strap Enablement

Strap Pins (see Note 1)			FS_OVERT* Function
ROM_50	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* Function ENABLED

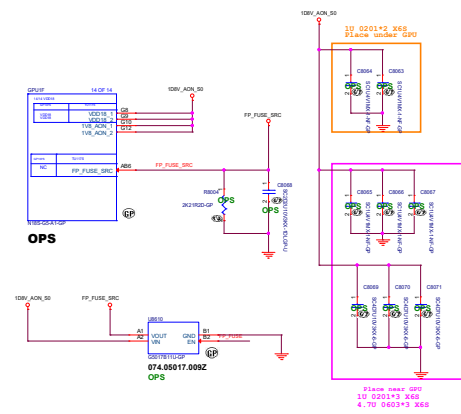
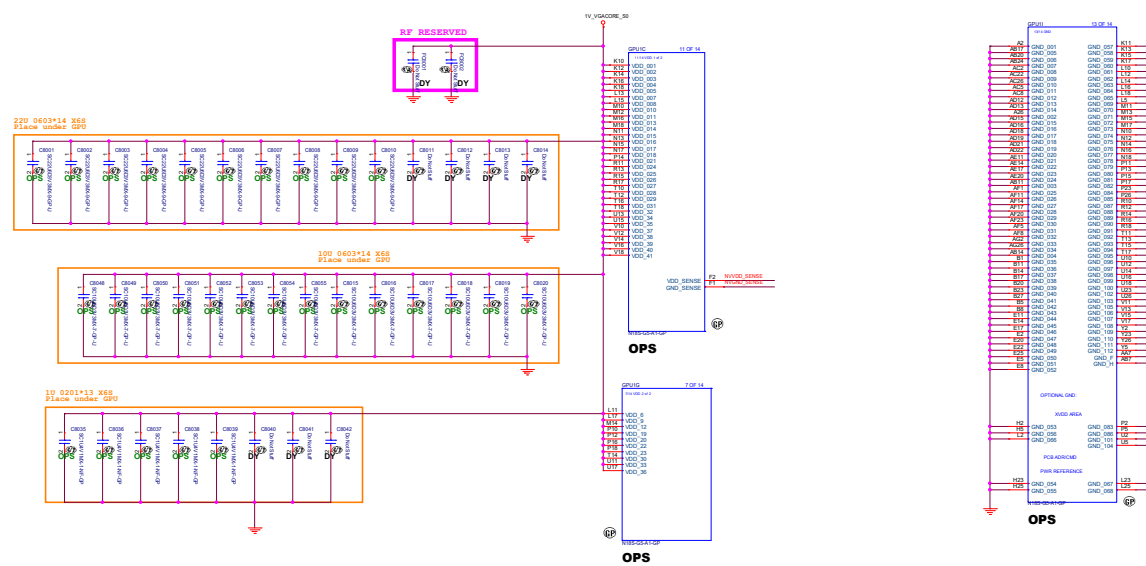
Table 12.5 SMB_ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins (see Note 1)						Functions Selected by This Strapping
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

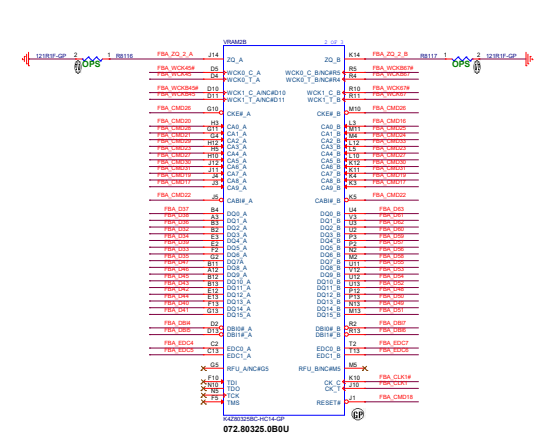
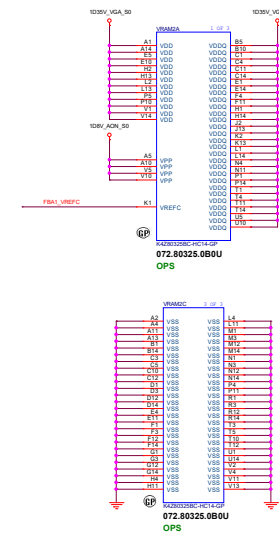
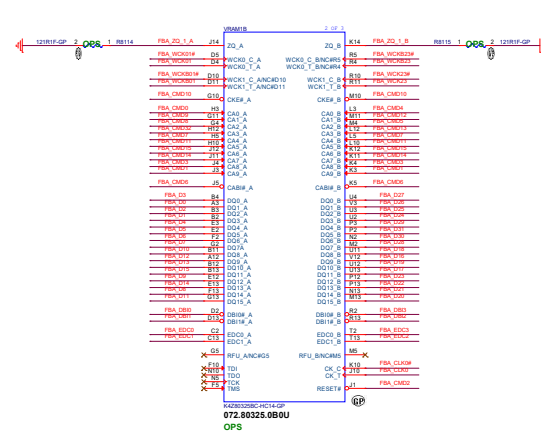
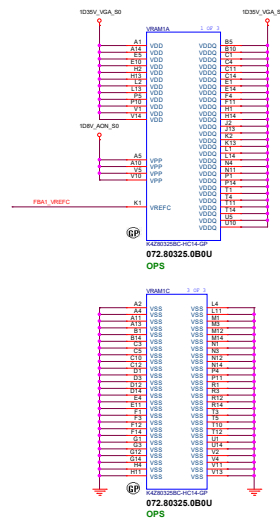
Strap Pin N18/0B2E-44

ROM_SI	Pull low to enable FS_OVERT*
ROM_50	
ROM_CLK	
STRAP5	+ SMB_ALT_ADDR
STRAP4	+ DEVID_SEL
STRAP3	+ PCIE_CFG
STRAP2	+ VGA_DEVICE
STRAP1	RAMCFG6[4:0]
STRAP0	

Note:
The ROM_50 pin should be pulled low using a 10 kΩ resistor for N18/0B2E-44 GPUs and using a 100 kΩ resistor for N17/0B2D-44/0B2C-44 GPUs.



www.teknisi-indonesia.com



8.2.2.14 GDORAM VREFC
GDORAM DRAMs include an integrated VREFC (VREF for DQ07 and ADDR). Figure 8.8 illustrates use of the integrated VREFC for x16 mode GDORAM DRAMs. Refer to the reference schematics for final layout values.

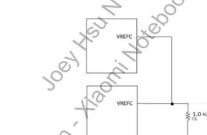
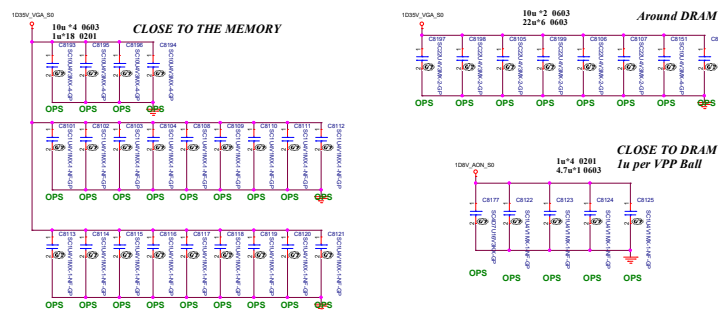


Figure 8.8 Use of Integrated VREFC for x16 Mode

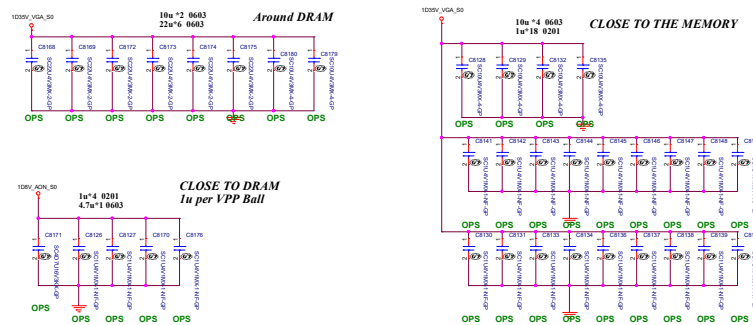
FOR VRAM1

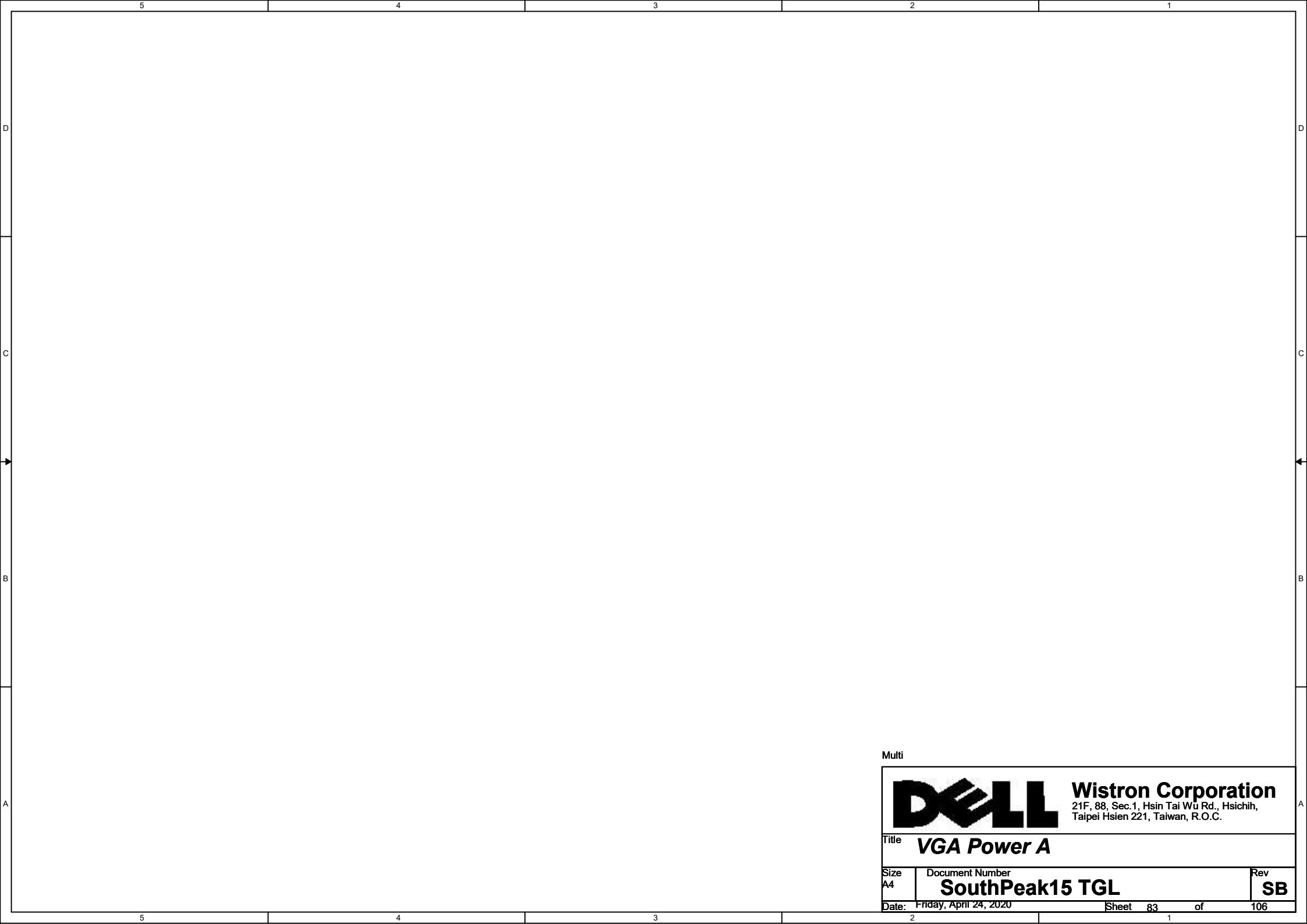
PLACE 0201 1uF UNDER MEMORY AS MUCH AS POSSIBLE



FOR VRAM2

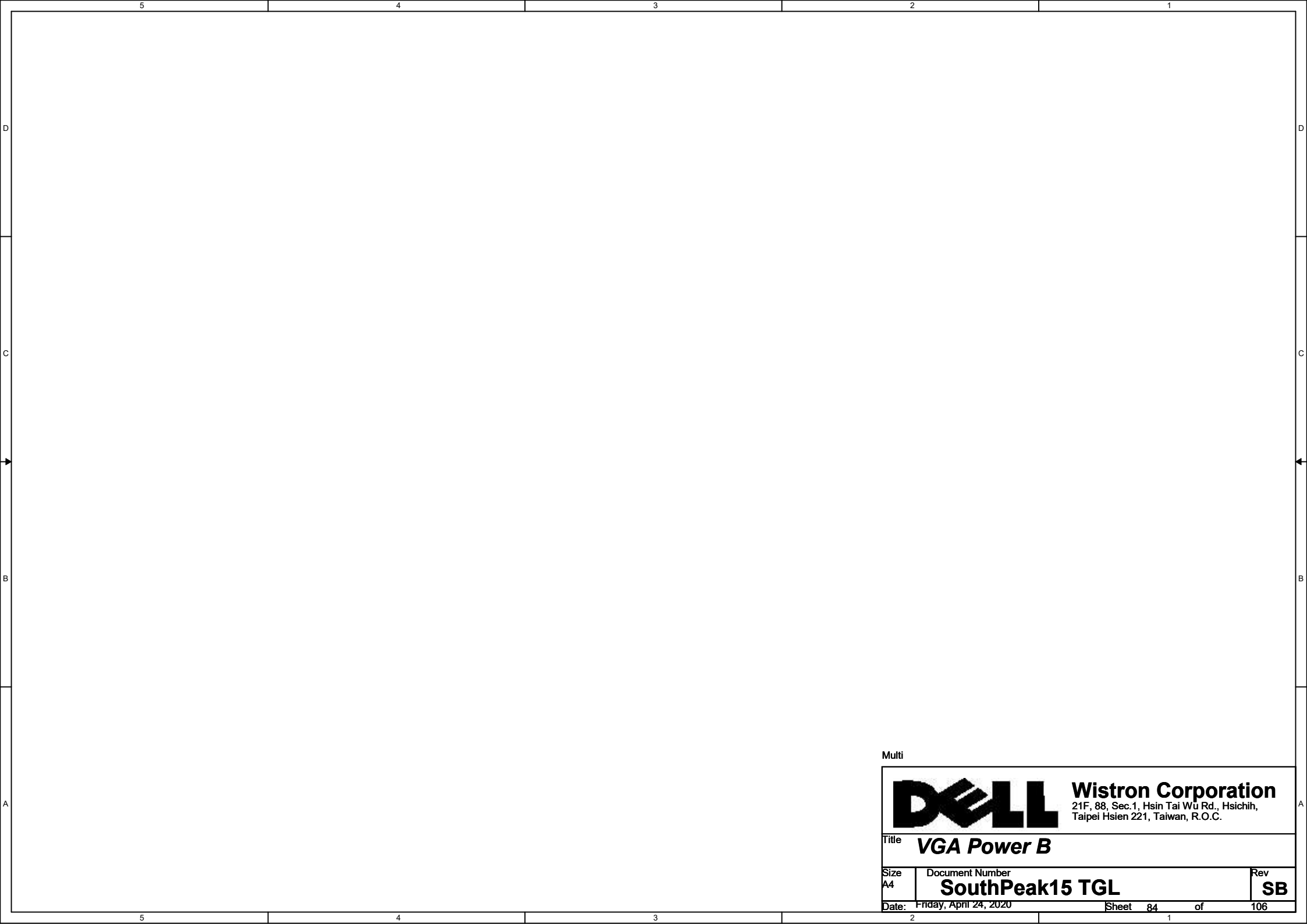
PLACE 0201 1uF UNDER MEMORY AS MUCH AS POSSIBLE





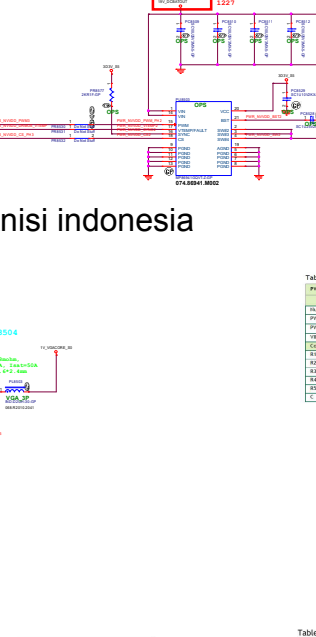
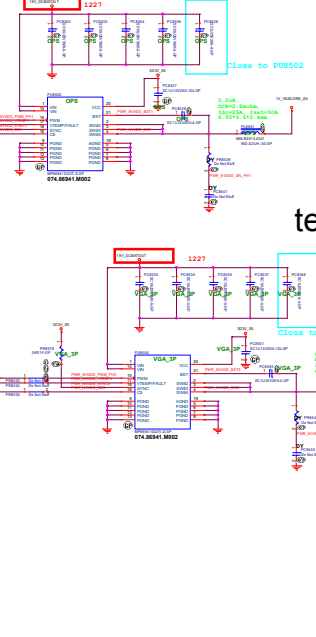
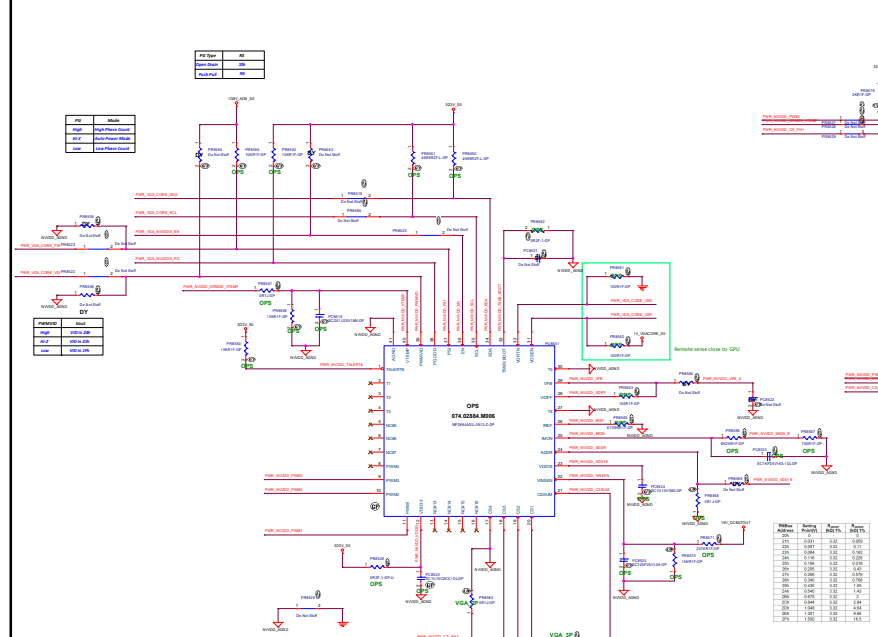
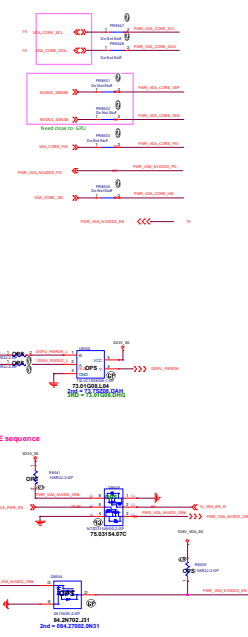
Multi

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title VGA Power A					
Size A4		Document Number SouthPeak15 TGL			Rev SB
Date: Friday, April 24, 2020		Sheet 83		of 106	



Multi

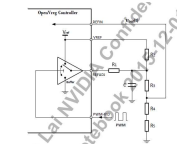
			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title VGA Power B					
Size A4		Document Number SouthPeak15 TGL			Rev SB
Date: Friday, April 24, 2020		Sheet 84 of 106			



teknisi indonesia

Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification	Units	Config
Number of Voltage Levels N	Level	100
PWM Frequency F _{PWM}	MHz	6.25
PWM Minimum Pulse Width T _{min}	ns	5.26
VID Transient Time T	ns	200
Component Value		
R1 (1%)	kΩ	6.19
R2 (1%)	kΩ	20.3
R3 (1%)	kΩ	4.32
R4 (1%)	kΩ	16.5
R5 (1%)	kΩ	8.20
C	μF	



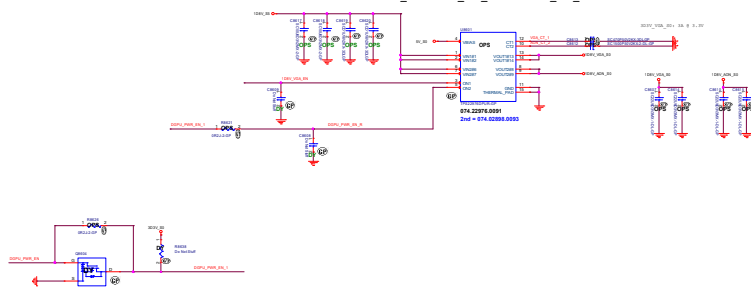
PWM-VID Specification		
		Config
V _{min}	V	0.3
V _{max}	V	1.3
V _{boot}	V	0.8
Voltage Step V _{step}	mV	6.25
Number of Voltage Levels N	level	160
PWM Frequency F _{PWM}	kHz	675
PWM Minimum Pulse Width T _{min}	ns	9.26
VID Transient Time T	us	1000
Component Value		
R1 (1%)	kΩ	6.19
R2 (1%)	kΩ	20.5
R3 (1%)	kΩ	4.32
R4 (1%)	kΩ	16.5
R5 (1%)	kΩ	8.20
C	μF	

Location	VGA_3P	VGA_2P
PC8530	Stuff	DY
PC8531	Stuff	DY
PC8533	Stuff	DY
PC8534	Stuff	DY
PC8535	Stuff	DY
PC8537	Stuff	DY
PC8546	Stuff	DY
PL8503	Stuff	DY
PR8578	Stuff	DY
PL8504	Stuff	DY
PR8573	Stuff	DY
PR8583	DY	Stuff

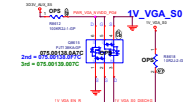
Main Func = dGPU

(DE-97158-001 Rev03) Power Up Sequence
 1. 3V with 800MHz (VGA_CORE) with 100V_VGA_S0 (1.50V) with 800MHz (1.50V)

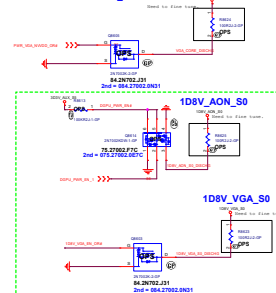
3D3V_S0 to 3V3_AON_S0 and 3D3V_VGA_S0



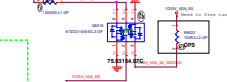
dGPU Power Discharge Circuit



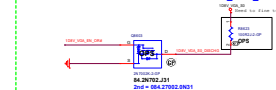
VGA_CORE



1D35V_VGA_S0

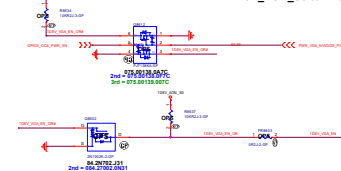


1D8V_VGA_S0

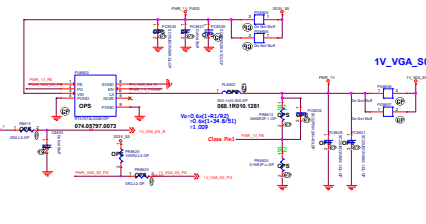
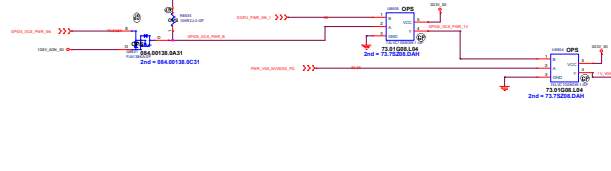


RT5797 for 1V_VGA_S0

1D8V_AON_S0 to 1D8V_VGA_S0

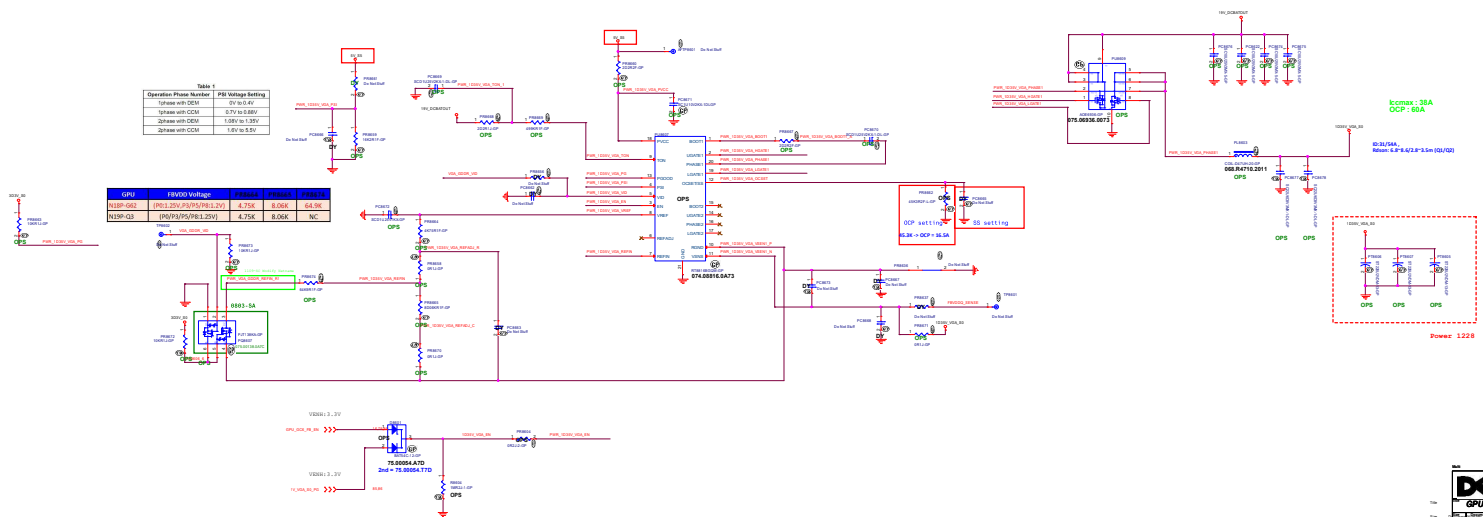


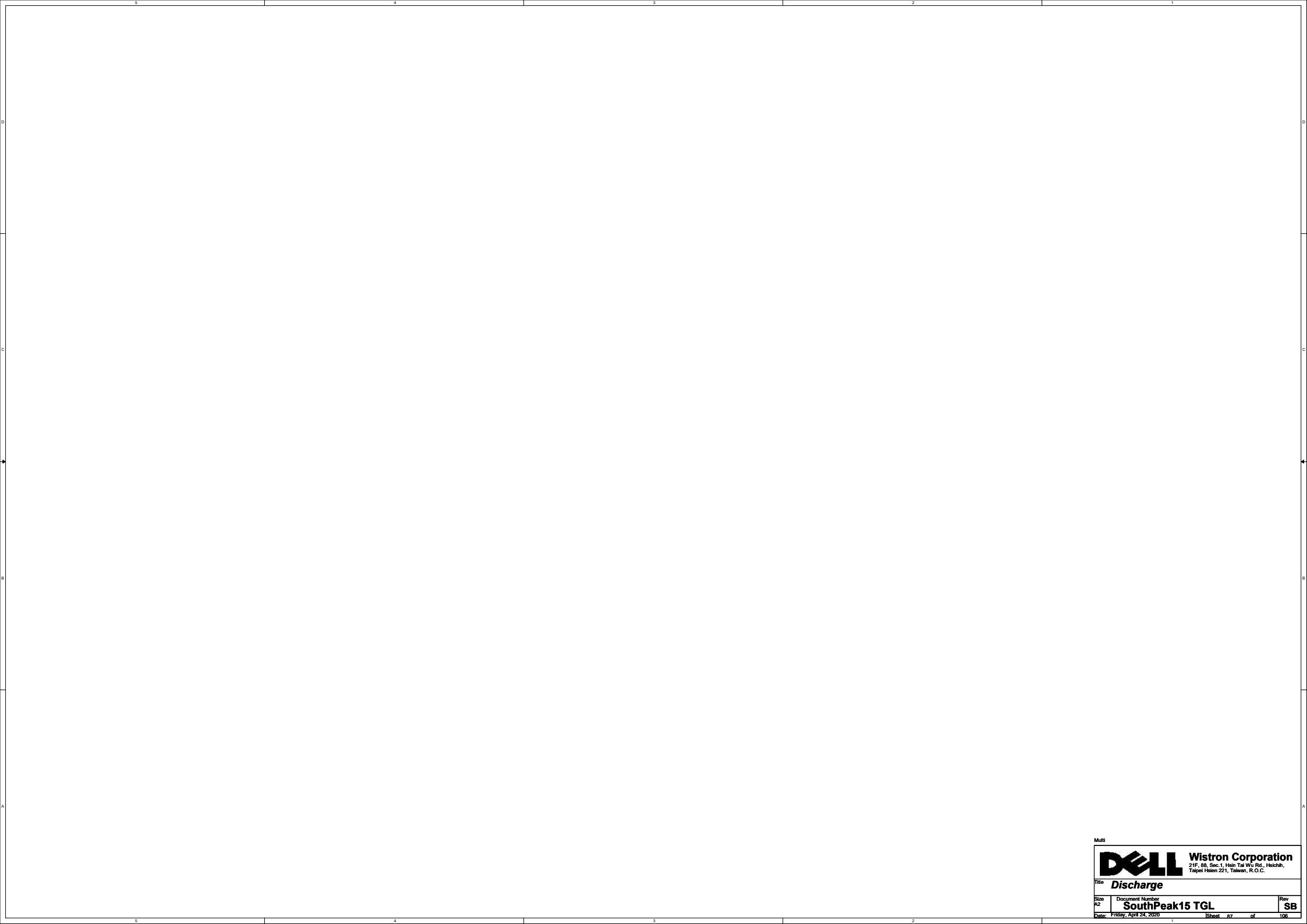
For tuning VGA_CORE sequence



Operation Phase	Monitor	PM Voltage Setting
1. Standby with CCM	0.7V to 0.8V	
2. Standby with CCM	0.7V to 0.8V	
3. Standby with CCM	0.7V to 0.8V	
4. Standby with CCM	0.7V to 0.8V	

GPU	FBW00 Voltage	FBW00 Voltage	FBW00 Voltage	FBW00 Voltage
1080P/60Hz	1.00V (VGA_CORE)	1.00V (VGA_CORE)	1.00V (VGA_CORE)	1.00V (VGA_CORE)
1080P/60Hz	1.00V (VGA_CORE)	1.00V (VGA_CORE)	1.00V (VGA_CORE)	1.00V (VGA_CORE)
1080P/60Hz	1.00V (VGA_CORE)	1.00V (VGA_CORE)	1.00V (VGA_CORE)	1.00V (VGA_CORE)





Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Discharge			
Size A2	Document Number SouthPeak15 TGL		Rev SB
Date: Friday, April 24, 2020 Sheet 87 of 108			

5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

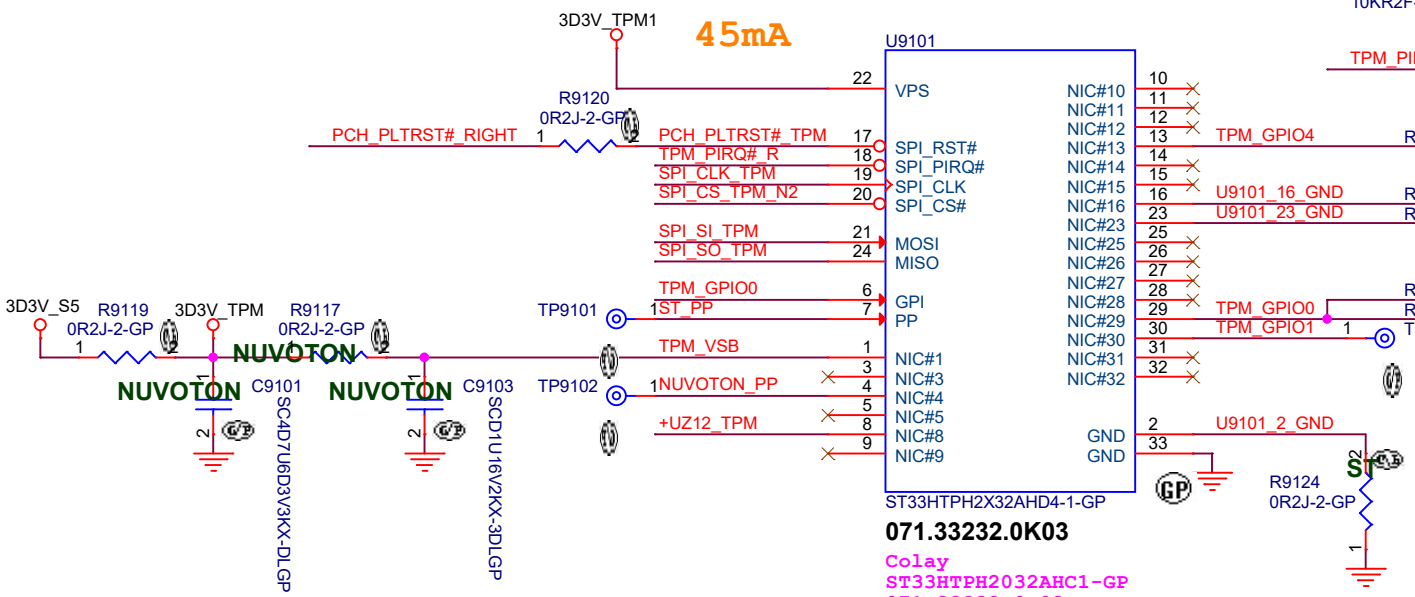
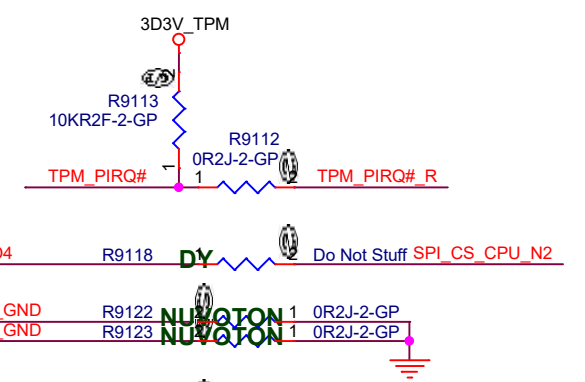
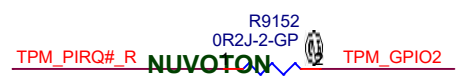
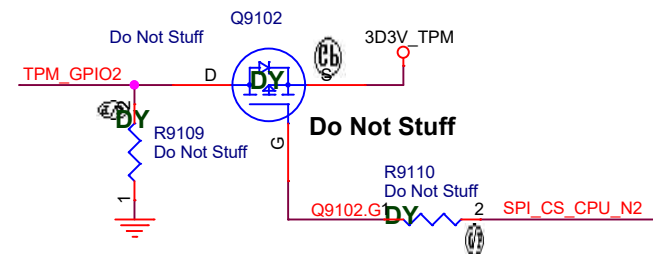
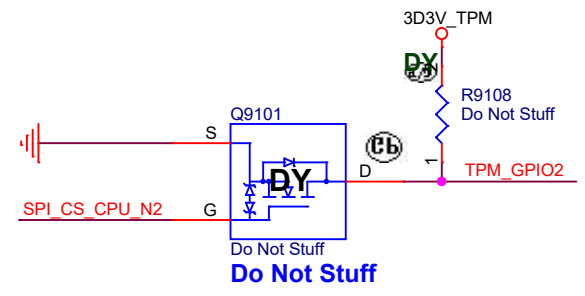
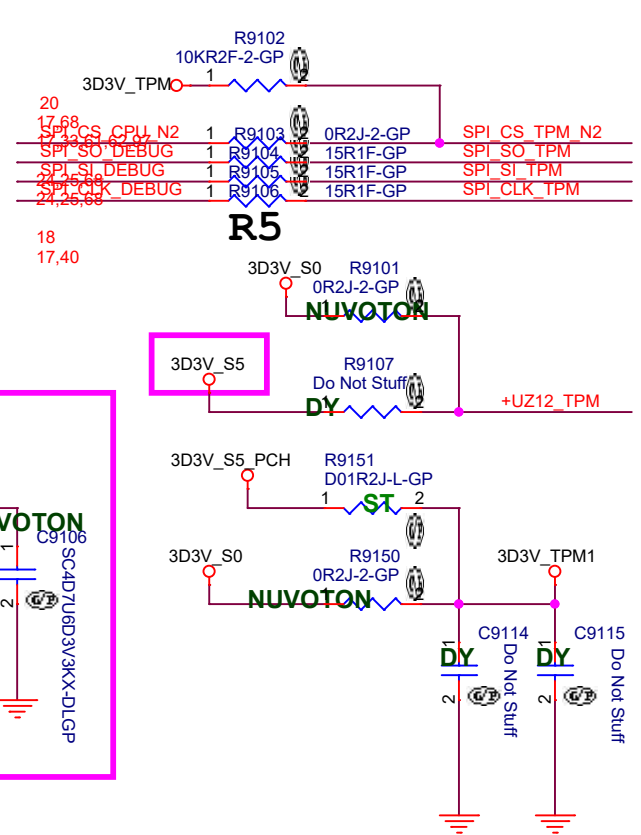
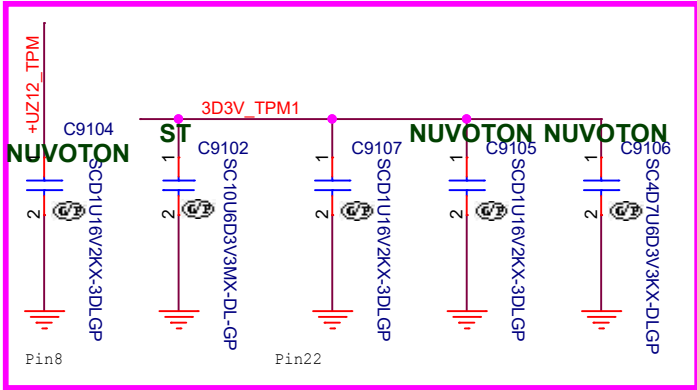
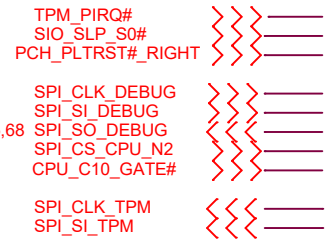
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title UNUSED PARTS (RSVD)			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 88 of	106

5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title INT IO (RSVD) (NFC)			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 90 of	106

Main Func = TPM



Multi

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

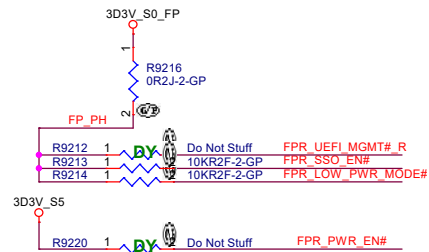
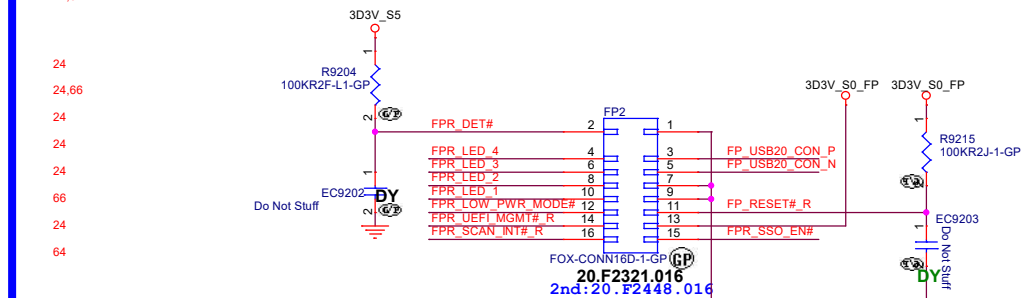
Title **INT IO (TPM)**

Size A4	Document Number	Rev SB
------------	-----------------	-----------

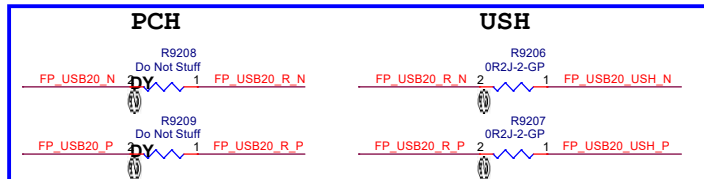
Date: Friday, April 24, 2020 Sheet 91 of 106

Main Func = Finger Printer

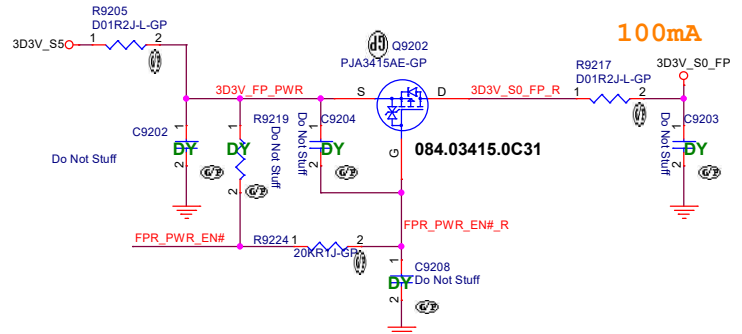
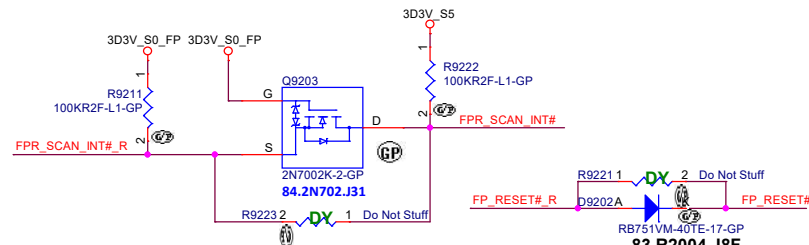
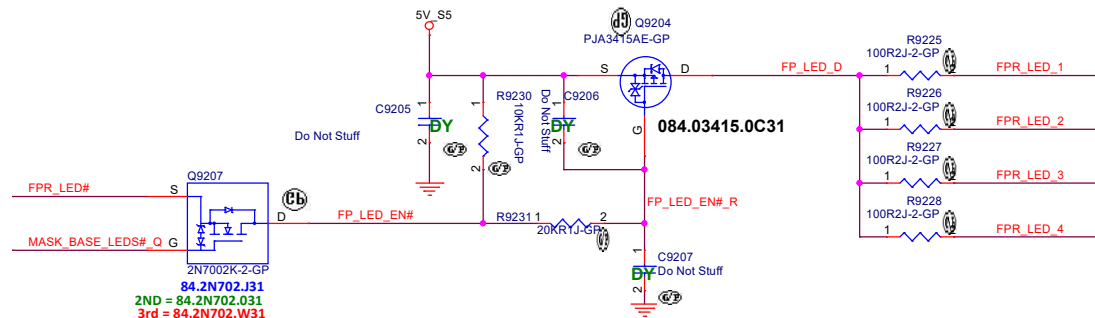
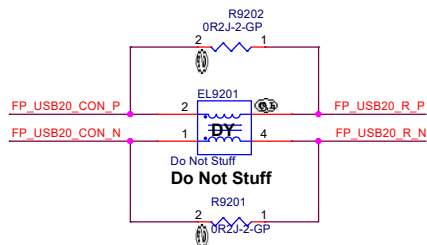
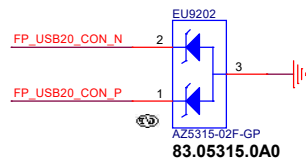
FP_USB20_P	<<>>	
FP_USB20_N	<<>>	
FPR_DET#	<<<<	24,64
FP_USB20_USH_N	<<>>	
FP_USB20_USH_P	<<>>	
FPR_PWR_EN#	>>>>	24
FPR_SCAN_INT#	<<<<	24,66
FPR_SSO_EN#	>>>>	24
FPR_UEFI_MGMT#_R	>>>>	24
FPR_LOW_PWR_MODE#	>>>>	24
FP_RESET#	>>>>	66
FPR_LED#	>>>>	24
MASK_BASE_LEDS#_Q	>>>>	64



Try to co-lay



www.teknisi-indonesia.com



5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title EXT IO (RSVD) (Express Card/PCIE slot)		
Size A4	Document Number	Rev SB
Date: Friday, April 24, 2020		Sheet 93 of 106

5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

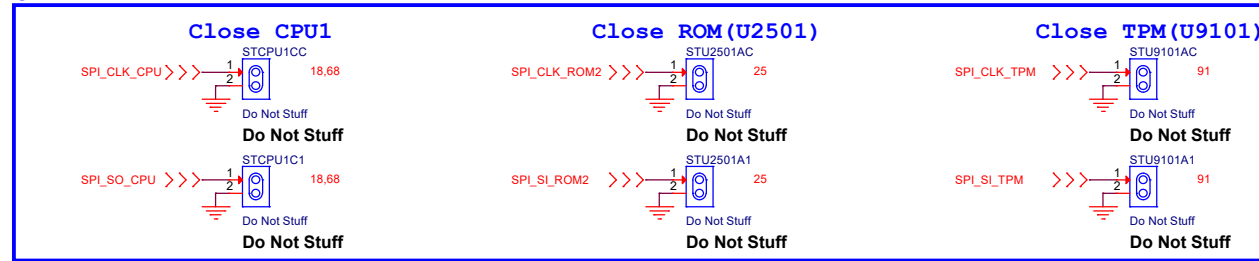
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title EXT IO (RSVD) (Smart Card/COM/PS2)		
Size A4	Document Number	Rev SB
Date: Friday, April 24, 2020		Sheet 94 of 106

5	4	3	2	1
D				
C				
B				
A				

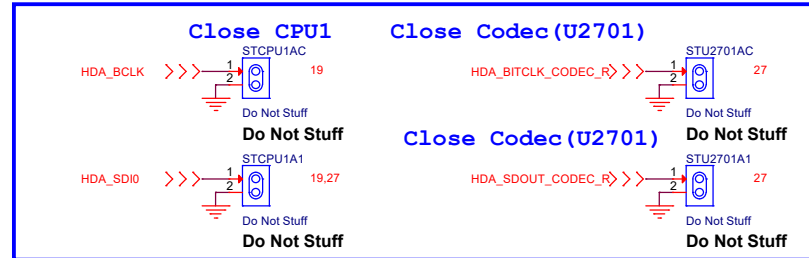
Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title EXT IO (RSVD) (Docking/LPT)			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 95 of	106

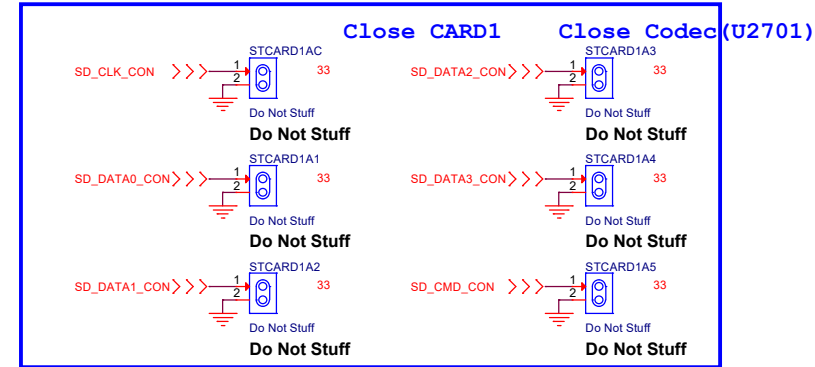
SPI



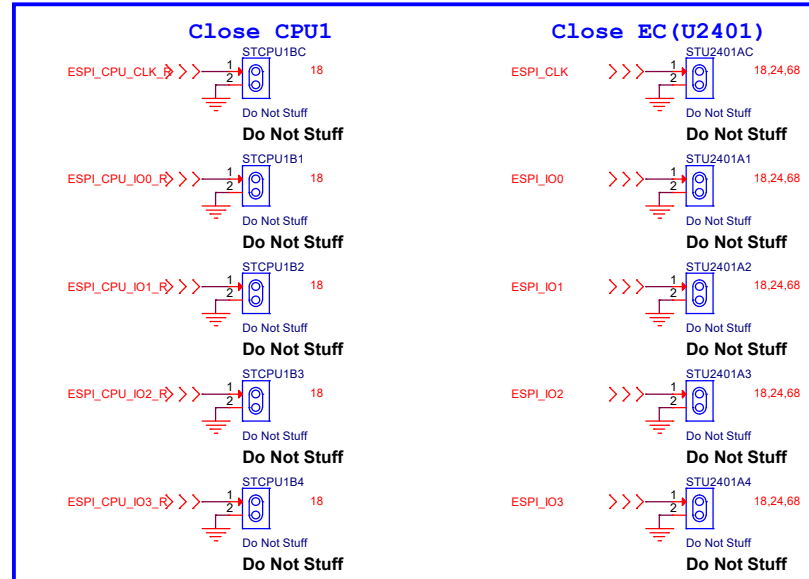
HDA



SDIO



ESPI



Multi

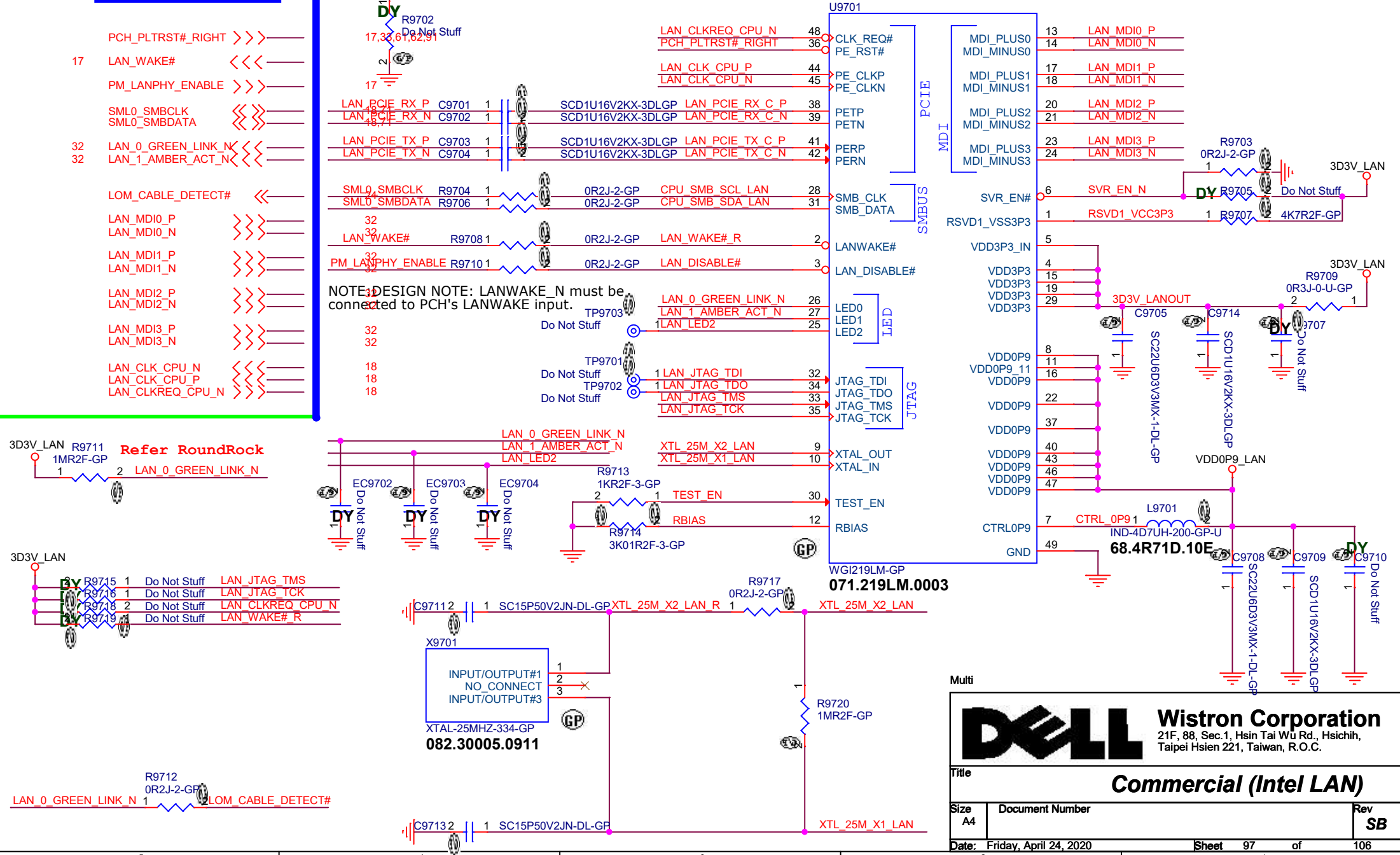
Main Func = LAN

LAN

16LAN_PCIE_RX_N
16LAN_PCIE_RX_P
16LAN_PCIE_TX_N
16LAN_PCIE_TX_P

PCH_PLTRST#_RIGHT >>>
17 LAN_WAKE# <<<
PM_LANPHY_ENABLE >>>
SML0_SMBCLK <<<
SML0_SMBDATA <<<
32 LAN_0_GREEN_LINK_N <<<
32 LAN_1_AMBER_ACT_N <<<
LOM_CABLE_DETECT# <<<
LAN_MDI0_P <<<
LAN_MDI0_N <<<
LAN_MDI1_P <<<
LAN_MDI1_N <<<
LAN_MDI2_P <<<
LAN_MDI2_N <<<
LAN_MDI3_P <<<
LAN_MDI3_N <<<
LAN_CLK_CPU_N <<<
LAN_CLK_CPU_P <<<
LAN_CLKREQ_CPU_N <<<

DESIGN NOTE: LAN_DISABLE_N must be connected to PCH's GPIO/LANPHYPC output. This GPIO pin must be set as "LANPHYPC" function through FITC tool. The signal does not require pull-up. R15 resistor is no-stuff default (for testing purpose).



Multi



Title			Commercial (Intel LAN)	
Size	A4	Document Number	Rev	
Date	Friday, April 24, 2020	Sheet	97	of 106

5	4	3	2	1
D				D
C				C
B				B
A				A

Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Commercial (LAN Switch)			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 98 of	106

R9917
 0R1J-GP
 DBG_PMODE 1 2 XDP_ITP_PMODE
 DEBUT

Pull high on Page15

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <i>Debug (XDP debug)</i>	
Size A4	Document Number SouthPeak15 TGL
Rev SB	
Date: Friday, April 24, 2020	Sheet 99 of 106

Table of Content

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
 For the value, it can be read by the number before R. (R means resistor)
 For the tolerance, it can be read from the last letter.
 For the rating, we don't show on the symbol name.
 For the size, R2=>0402, R3=>0603, R5=>0805,.....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
 Capacitor type + value + rating + size + tolerance + material
 SCD1U10V2MX-1
 SC=> SMT Ceramic, TC=> POS cap or SP cap
 D1U => 0.1uF
 10V => the voltage rating is 10V
 2=> 0402, 3=>0603, 5=>0805
 M=>tolerance M, K, Z
 X=> X7R/X5R, Y=> Y5V
 -1 => symbol version, nonsense to EE characteristic

Multi



Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title

Table of Content

Size

A4

Document Number

Rev

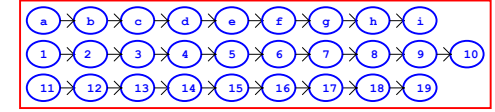
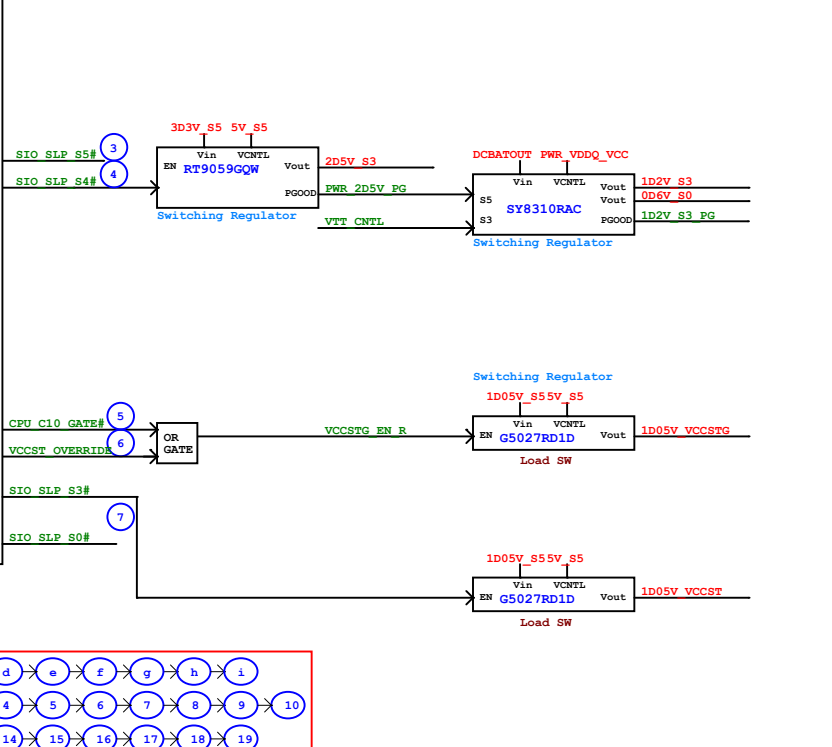
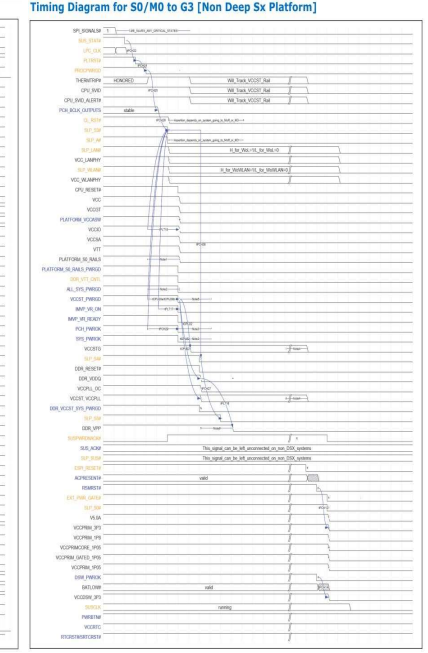
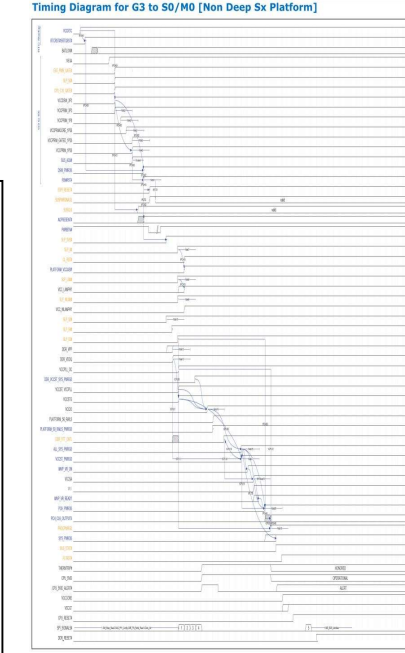
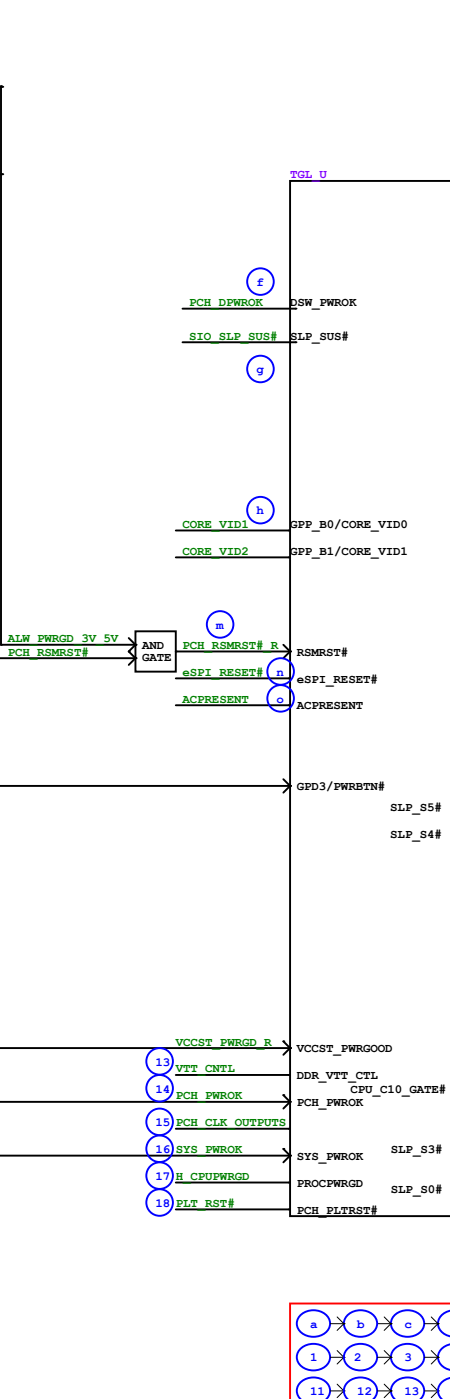
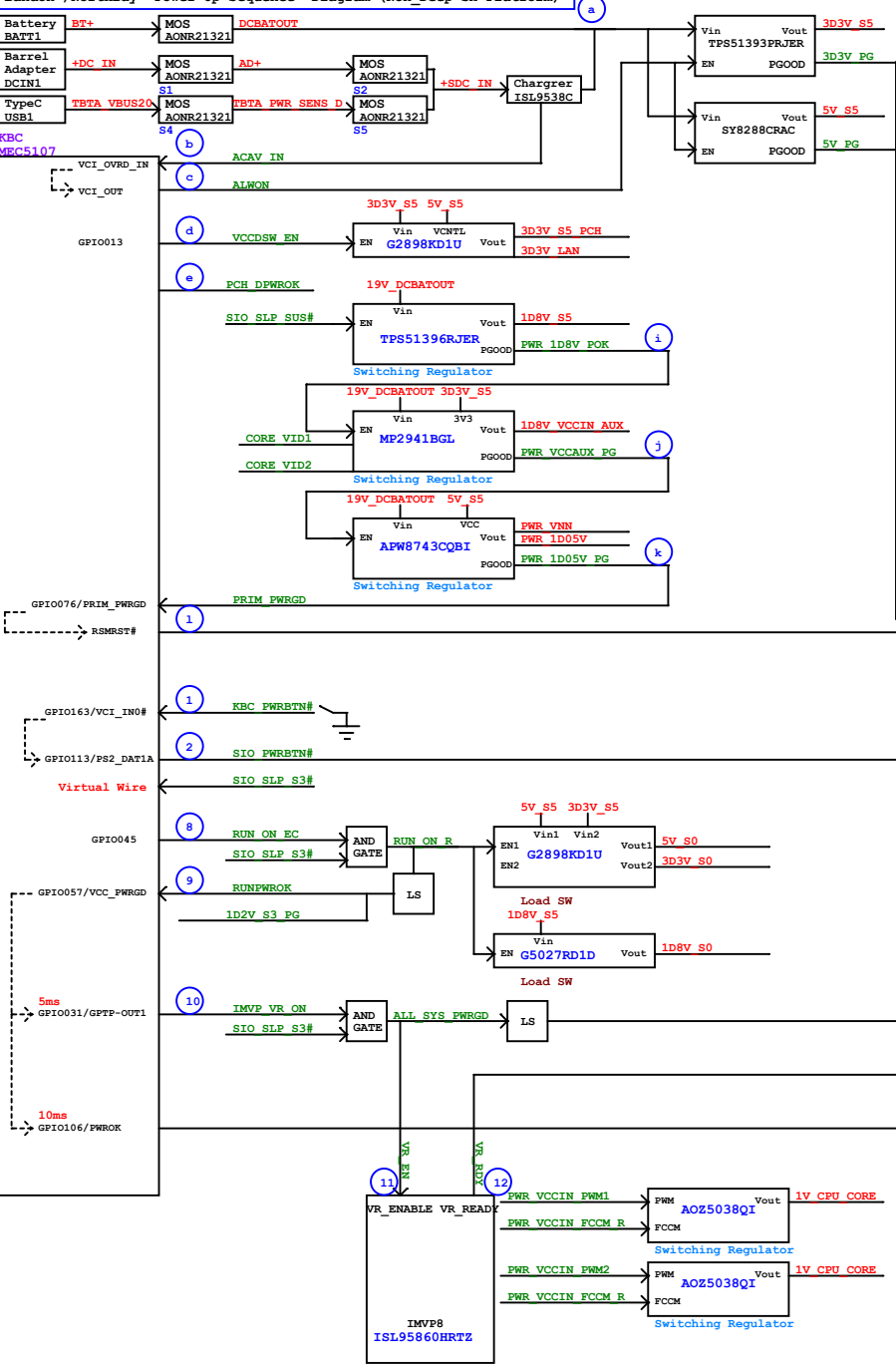
SB

Date: Friday, April 24, 2020

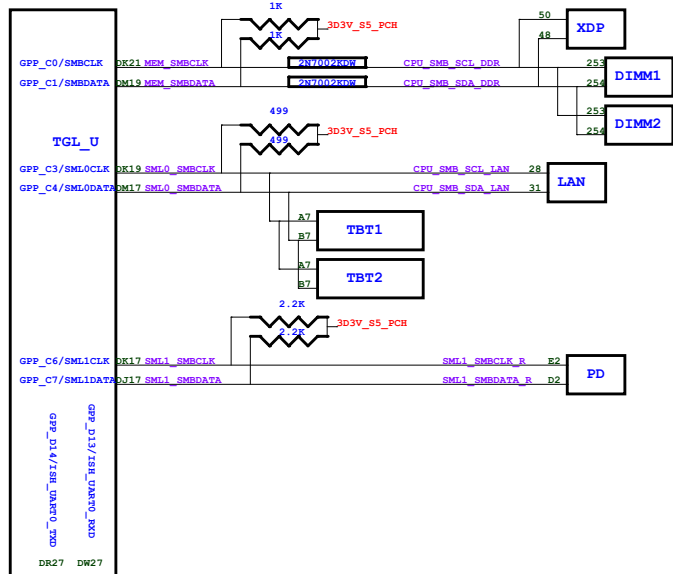
Sheet 100 of 106

[illegible]

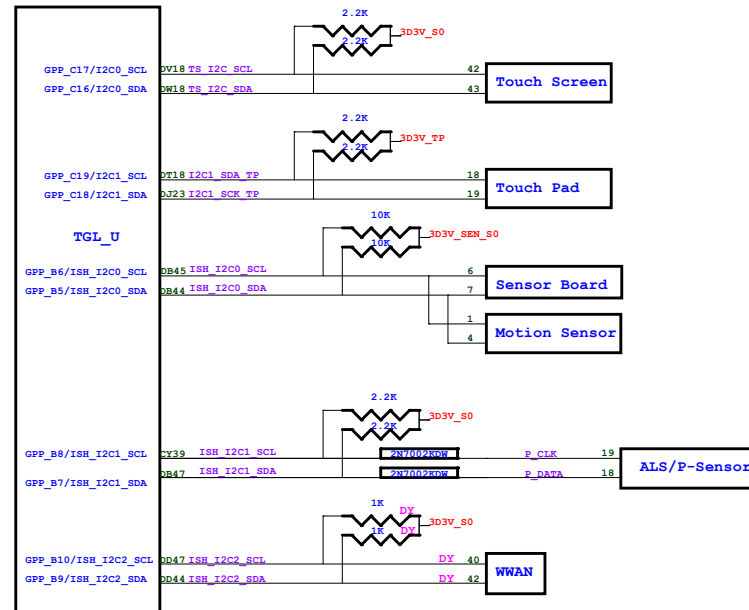
Bandon /NorthBay Power Up Sequence Diagram (Non_Deep Sx Platform)



SMBus Block Diagram



I2C Block Diagram



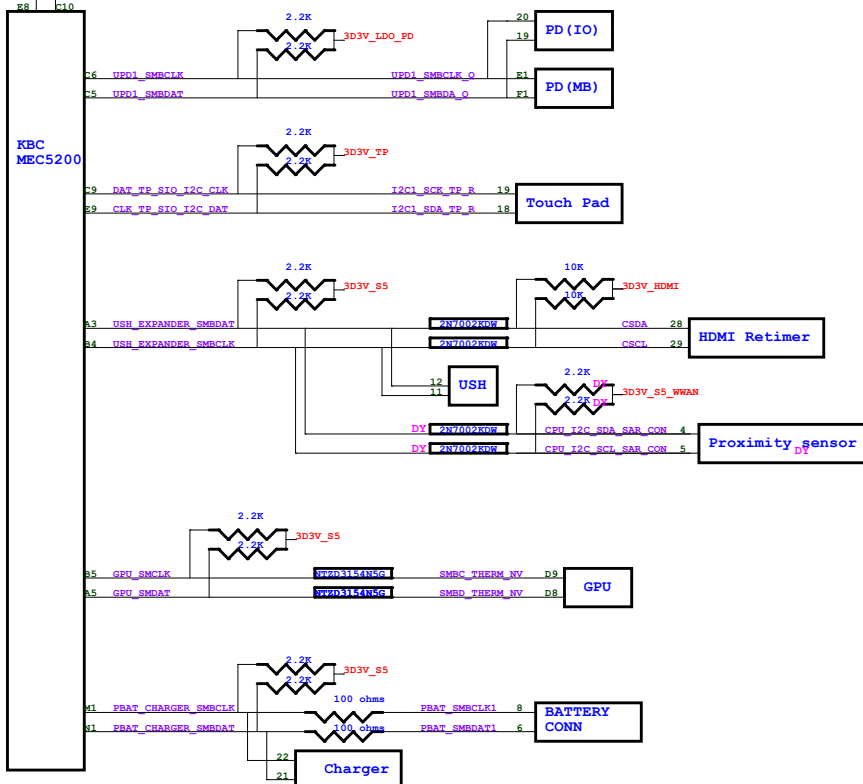
LAN DATASHEET

Pin Name	Pin #	Type	Op Mode	Notes and Functions
SMB_CLK	28	CIN	Bi-dir	SMBus clock. Pull this signal up to 3.3 Vdc (auxiliary supply) through a 4950 resistor (unless in the module).
SMB_DATA	31	CIN	Bi-dir	SMBus data. Pull this signal up to 3.3 Vdc (auxiliary supply) through a 4950 resistor (unless in the module).

Table 6-103. Bus Capacitance/Pull-Up Resistor Relationship

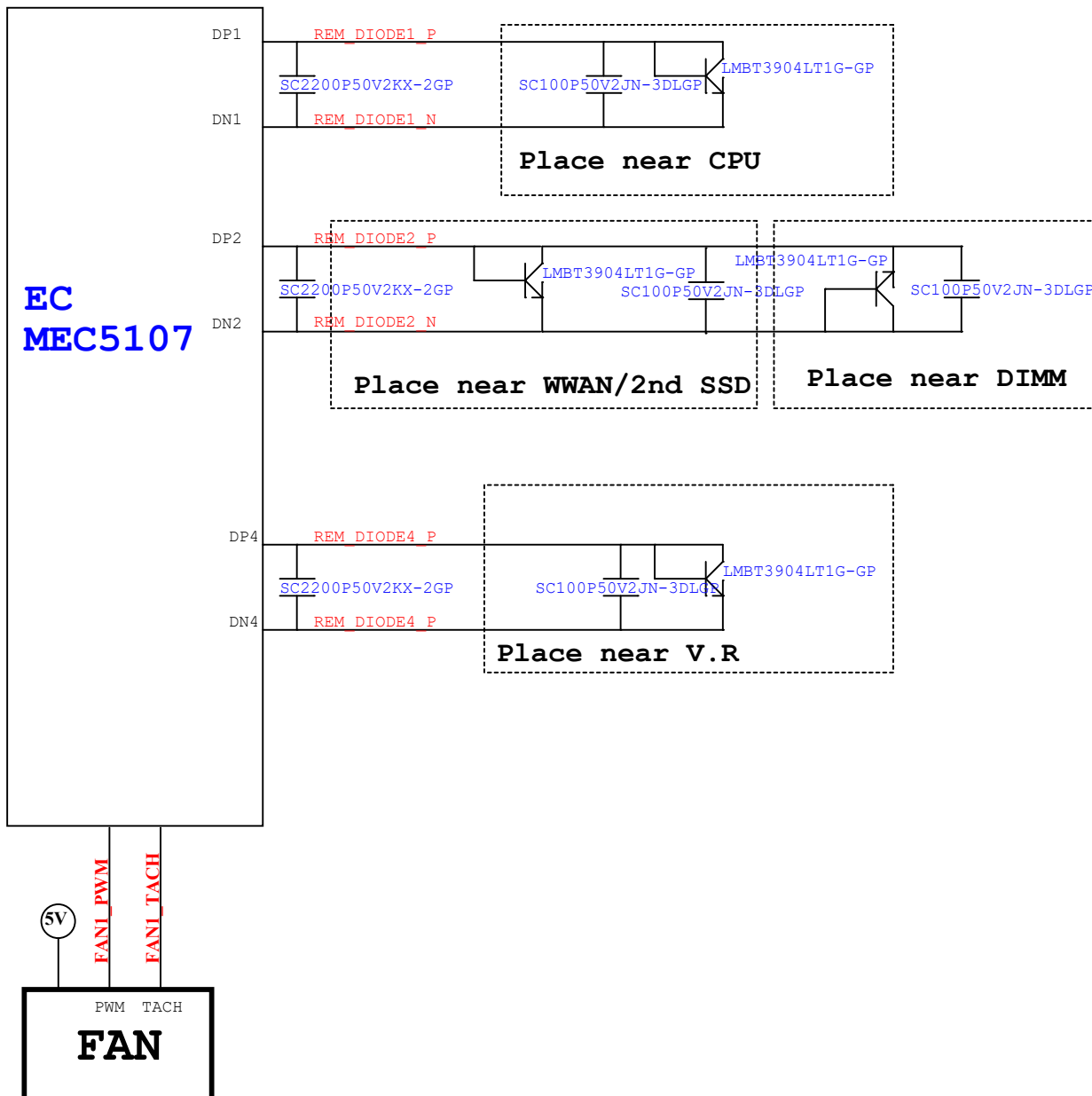
Standard Mode (100kHz) - Pull-up / Pull-down Resistor Settings		
Total Bus Capacitance (C _b)	External Pull-up	PCH Pull Down Strength (Refer EDS)
Upto 400 pF	2.2KΩ	100Ω
Fast Mode (400kHz) - Mode Pull-up / Pull-down Resistor Settings		
Total Bus Capacitance (C _b)	External Pull-up	PCH Pull Down Strength

Upto 100pF	2.7KΩ	100Ω
Upto 200pF	1.5KΩ	
Upto 300pF	1KΩ	
Upto 400 pF	680Ω	
Fast mode Plus (1MHz) - Pull-up/down strength Settings		
Total Bus Capacitance (C _b)	External Pull-up	PCH Pull Down Strength
Upto 50pF	2.2KΩ	100Ω
Upto 100pF	1.2KΩ	
Upto 200pF	560Ω	
Upto 300pF	390Ω	
Upto 400 pF	270Ω	420Ω

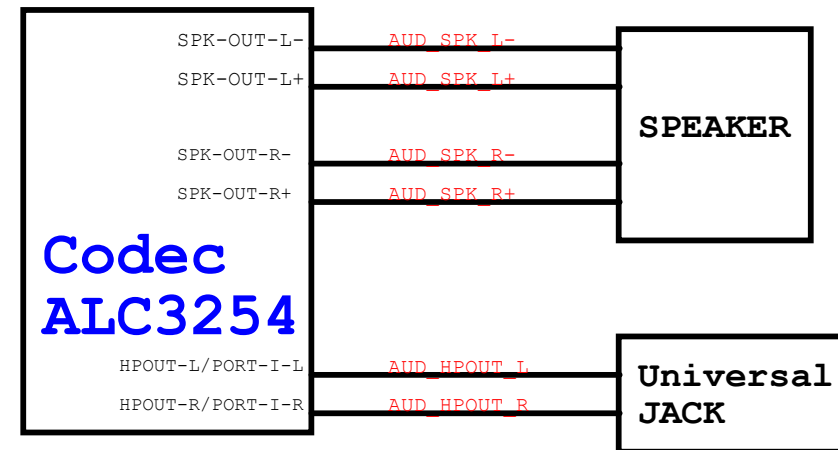


Multi

Thermal Block Diagram

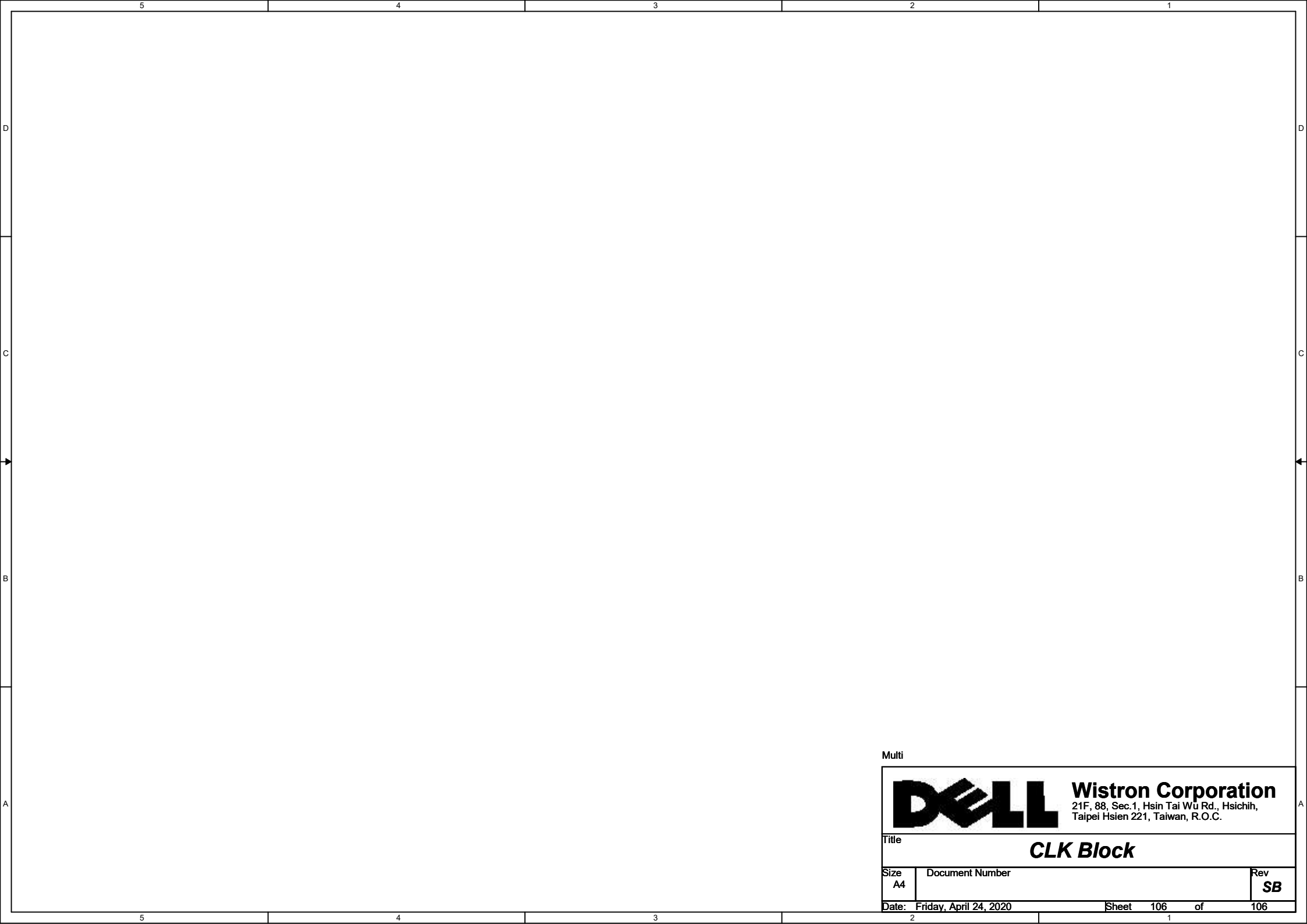


Audio Block Diagram



Multi

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title THERMAL/AUDIO BLOCK DIAGRAM			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020	Sheet 105 of		106



Multi

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CLK Block			
Size A4	Document Number		Rev SB
Date: Friday, April 24, 2020		Sheet 106 of	106